GROWTH AND CHARACTERIZATION OF DIELECTRIC MATERIALS FOR WIDE BANDGAP SEMICONDUCTORS

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
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For my family, and all those who want to believe

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GROWTH AND CHARACTERIZATION OF DIELECTRIC MATERIALS
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Dielectric materials for gate application on wide bandgap semiconductors were studied in this dissertation. These dielectric materials must operate at high temperatures and under high power loads. For this, the selected dielectric materials must be thermally stable to temperatures above 1000°C for device fabrication, chemically stable to prevent diffusion into the semiconductor, and have a low defect density to reduce the charged trap sites in the dielectric and at the dielectric/semiconductor interface. Four dielectric materials were investigated: aluminum nitride (AlN), gallium oxide (Ga_2O_3), gadolinium oxide (Gd_2O_3), and magnesium oxide (MgO).

These materials were deposited by using molecular beam epitaxy (MBE) where the individual elements are supplied independent of each other. This technique allows for use of a wide range of growth conditions in order to obtain the highest quality material. The dielectrics were first deposited on silicon substrates and characterized to obtain

general growth conditions. Then, the wide bandgap semiconductors were investigated for the final results and device fabrication. Growth initiation experiments were performed to determine a proper starting procedure for the attainment of high quality material. The samples were characterized using a wide variety of techniques to determine the surface roughness, crystal structure, chemical composition and electrical properties.

Aluminum nitride grown on silicon carbide at 325°C gave the best results of the dielectric materials produced. Current-voltage measurements showed a breakdown field strength of 6.8 MV/cm and indicated that there were no memory affects at elevated temperature device operation. Good quality gallium oxide was difficult to obtain due to its weak bonding to the semiconductor and the large variation in chemical composition of the as deposited films. Gadolinium oxide showed promise as a dielectric material and was thermally stable up to 1000°C as shown in AFM, AES, and x-ray diffraction. However, the Gd_2O_3 only had a breakdown field strength of 0.73 MV/cm when grown on gallium nitride. This was attributed partly to a high defect density within the material and partly to the roughness of the starting GaN surface. The magnesium oxide showed similar results to the gadolinium oxide with a breakdown field strength of 0.68 MV/cm, but again, this is due in part to the rough GaN surface.

CHAPTER 1
INTRODUCTION

1.1 Motivation

Microelectronic devices based on silicon constitute about 95% of the solid-state market today. The remaining 5% of the market consists of compound semiconductors. These compounds are based on elements from group III and group V from the periodic table and the majority of these compounds are based on gallium arsenide (GaAs) and indium phosphide (InP). These compound semiconductor devices have higher carrier mobilities, resulting in faster devices, and a lower saturation electric field, producing smaller power delay, than silicon. Also, some compounds have direct bandgaps that lead to efficient light emission and light detecting. This is a field that silicon will never occupy since its bandgap is indirect.

Transistor research based on compound semiconductors has led to several breakthroughs in device performance. It was not until recently that research in this field produced a GaAs metal/oxide/semiconductor (MOS) capacitor that demonstrated properties useful for transistors.[1] This discovery has lead to an operational GaAs based MOS transistor incorporating gallium gadolinium oxide as a gate dielectric.[2] Further research has shown that the gadolinium content of the oxide was responsible for surface passivation and improved dielectric properties.[3,4,5,6,7] There are, however, limits to these exciting compound materials such as thermal operating limits and power handling

capabilities. A new breed of compound semiconductors has come into the light of science, from the darkness of science fiction. These new semiconductors are termed wide bandgap.

Wide bandgap semiconductors have been researched for decades. It began with silicon carbide (SiC) in the middle part of the 20th century. In more recent decades, research has expanded to include wide bandgap compounds consisting of elements from group III and nitrogen, denoted as III-nitrides, and elements from group II and group VI, denoted as II-VI's. The latter has gone the way of the Coelacanth, forgotten but not lost. Table 1 lists some wide bandgap semiconductors and their properties, as well as silicon and gallium arsenide. The term wide bandgap refers to the forbidden energy gap of a material, a region in the energy diagram that is not occupied by electrons, that is typically greater than 2eV, as shown in Figure 1.1. Of the III-nitride materials, gallium nitride (GaN) has become the most widely studied. The III-nitrides and SiC have become the mainstay for the wide bandgap semiconductor industry. Until recently, most of the wide bandgap research has been pointed toward the production of optical devices, mainly short wavelength (blue to ultra-violet) lasers and light emitting diodes (LEDs). This included research in material growth, dopant incorporation of both n and p type species, ohmic contact to both n and p type material, device isolation and processing. This research has led to the development of 10000 hour blue laser diodes based on GaN.[8] This has been possible largely due to the fact that the GaN and SiC materials exhibit excellent thermal stability during device operation.

From the laser research, studies have been initiated to create microwave and ultra-high power switches. The main advantage to using GaN and SiC for power devices is the

high thermal stability and large band gap. Advances in SiC and GaN have led to power switches based on different configurations like metal-semiconductor field effect transistors (MESFETs), heterojunction field effect transistors (HJFETs), thyristors and heterojunction bipolar transistors (HBTs). [9,10,11,12,13,14]

While these devices have shown promise for a number of applications, the metal oxide (or insulator) semiconductor field effect transistor (MOSFET or MISFET) is also a desirable structure. The MOS(MIS)FET structure has advantages over the heterjunction type transistor due to its relative insensitivity to temperature during operation. The thermal limits of the MESFET structure are between 300°C to 600°C, which gives that device an upper operating limit. Also at these temperatures, there is the possibility of forming metal gallides and silicon nitride with the GaN interface at prolonged heating. The MOSFET structure can be made with either n-type or p-type material under the gate. The use of both n-MOSFET and p-MOSFET on the same chip results in a complementary device structure, known as c-mos. Complementary devices are required for logic circuits. A complementary circuit structure based on wide bandgap semiconductors will allow for an entire monolithic control circuit to be constructed for high temperature/high power use. However, for a MOS(MIS)FET to be realized, a high quality dielectric material must be created for the gate insulator. This material must have a bandgap wider than the semiconductor, a larger dielectric constant than the semiconductor, and high temperature stability similar to the semiconductor. The materials that have been researched for this roll are discussed in section 2.2. Finding new materials to satisfy these requirements is the goal of this research. The materials selected

for this study are aluminum nitride, gallium oxide, gadolinium oxide, and magnesium oxide.

Table 1

Semiconductor	Structure	Lattice Constant (Å)	Bandgap (eV)	ε
Si	Cubic	A=5.43	1.11	11.8
GaAs	Cubic	A=5.65	1.35	12.8
SiC	3-Cubic 4-Hexagonal 6-Hexagonal	A=4.36 A=3.08,c=10.05 A=3.08,c=15.12	2.4 3.2 3.0	9.7 10 10
AlN	Hexagonal	A=3.112,c=4.982	6.2	8.5
InN	Hexagonal	A=3.548,c=5.760	1.89	15.3
GaN	Cubic Hexagonal	A=4.54 A=3.189,c=5.185	3.3 3.39	-- 8.9
ZnS	Cubic	A=5.41	3.6	8.9

1.2 Dissertation Outline

The objective of this study is to explore the feasibility of growing different dielectric materials on wide bandgap semiconductor material by molecular beam epitaxy and characterize that material.

The background and literature review are set out in chapter 2. In the background, definitions of dielectric materials, capacitance, and MOSFET are given. The literature

review contains descriptions and results of dielectric materials used on GaN and SiC. In chapter 3, the growth methods of the nitride and oxide dielectrics are explained, along with characterization methods used. Chapter 4 describes the results of the different dielectric materials grown and discusses how the different dielectric materials compare to each other. Capacitor results are given and some actual MOSFET results are also shown. The final conclusions and future experiments are defined in chapter 5.

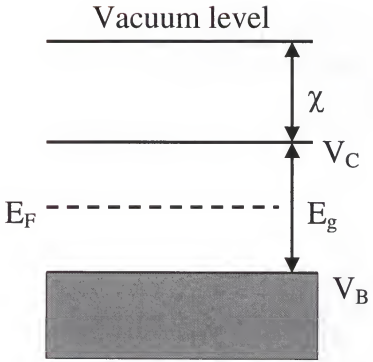


Figure 1.1 An energy band diagram. E_C is the conduction level, E_V is the valance level, E_F is the Fermi level, E_g is the energy band gap, and χ is the electron affinity.

CHAPTER 2
BACKGROUND AND LITERATURE REVIEW

2.1 Introduction to Dielectric Films, Capacitors, and MOS(MIS)FETs

In the following sections, the basic understanding of dielectric films, their properties, and applications are discussed. The capacitor becomes an important tool for testing these dielectric materials. The metal/insulator/semiconductor transistor is a solid-state switch that is controlled by the capacitor structure in the gate region.

2.1.1 Dielectric films

Insulators are characterized by the absence of charge transport. Insulators have positive and negative charges in the form of the atom nucleus and electron cloud, but these charges are bound to the atom or molecule and are not available for conduction. When materials are placed in an electric field, there is a shift, or polarization, in the charge distribution and it is this polarization that leads to dielectric behavior in the material.[15] The polarization induces dipoles within the atomic or molecular structures that are aligned with the applied field. The ability of a material to resist the polarization of charge is described as the dielectric constant, κ, which is the ratio of the permittivity of the material, ε_i, to the permittivity of vacuum, ε_v.

$$\kappa = \varepsilon_i / \varepsilon_v \qquad (2.1)$$

The dielectric constant can also be related to the internal field created within the material and the external field applied, through equation 2.2.[16]

$$E_{internal} = \frac{E_{applied}}{\kappa} \tag{2.2}$$

The polarization, P, of the material is related to the dielectric constant by equation 2.3, where ξ is the strength of the electric field (V/m). It can be assumed from this relation that the polarization increases as the electric field strength increases, until all the dipoles are aligned such that:

$$P=(\kappa-1)\varepsilon_o\xi \tag{2.3}$$

There are several applications for dielectric materials. Passivation of high voltage junctions, isolation of devices and interconnects and gate insulation of field effect transistors are a few that are relevant for this discussion. For a material to be a successful dielectric it must meet certain criteria. Desirable characteristics include: chemical stability over the life of the device, immobile charge traps (to avoid shorting and frequency limits) and a dielectric constant higher than that of the semiconductor (to avoid generating a high electric field in the dielectric). In the case of the wide bandgap semiconductor devices, the dielectric materials must also have excellent thermal stability, since the high power applications will result in elevated operating temperatures. The dielectric /semiconductor interface is also an important focus of research in the area of device processing. The interface state density of carrier traps must be $<10^{11}\ eV^{-1}cm^{-2}$ for a device to be considered successful. Another important focus is the fixed dielectric

charge density, or the carrier trap density within the dielectric. To date, there have been several dielectric materials researched for use in wide bandgap semiconductor switches. The list includes AlN, Al_2O_3, Ga_2O_3, $Ga_2O_3(Gd_2O_3)$, SiO_x, and Si_3N_4. The properties of these and other dielectric materials are given in Table 2.1.

Table 2.1

Material	Bandgap (eV)	Dielectric (ε)	Melting Point (K)	Ref.s
AlN	6.2	8.5	3273	17,18,19
Al_2O_3	5.75	12	2319	20,21,22
Ga_2O_3	4.4	10	2013	23,24,25
Gd_2O_3	5.3	11.4	2668	26,27,28
$Ga_2O_3(Gd_2O_3)$	4.7	14.2	2023	2,29
SiO_x	8-9	3.9	1993	30,31, 22
Si_3N_4	5.0	7.5	2173	30,31,32
MgO	7.3	9.8	3073	33,34,35,22

2.1.2 The metal/oxide/semiconductor capacitor

Since the gate is the actual on/off switch in the transistor structure, defining the properties of the gate and its operation are extremely important. The gate structure is identical to the metal/oxide/semiconductor capacitor, shown in figure 2.1. A capacitor is a device made of two parallel, conducting plates separated by an insulating material. When a direct current (dc) voltage is applied to one side of a capacitor, an equal and opposite charge is created on the other side of the capacitor. In most cases, the dc voltage

is applied to the metal side of the capacitor and the created charge is in the semiconductor. The amount of capacitance that the capacitor can hold is directly related to the dielectric constant of the dielectric material.[36] This is easily shown in equation 2.4, where C is the capacitance, ε_o is the permittivity of vacuum(ε_o=8.854x10^{-14} F/cm), ε_i is the permittivity of the material, A is the area of the metal contact, and d is the thickness of the dielectric material.

$$C=\varepsilon_o\varepsilon_i A/d \qquad (2.4)$$

The capacitance is independent of the applied voltage to the gate and is completely dependant on the geometry and the dielectric constant. This gives a theoretical capacitance for a given device geometry. If the applied electric field becomes too great, the charges are ripped from the material and conduct to the charged plates. This leads to a short in the material and is termed dielectric breakdown.

However, as in life, the theoretical value and the measured value seldom match. The measured capacitance value, using the apparatus described in section 3.2.8, is actually two capacitors in series. These are the dielectric capacitance and the semiconductor space-charge layer capacitance. The semiconductor capacitance ,C_s, is responsible for the deviation in the measured capacitance and is voltage dependant.[30] As the bias is applied to the metal, the majority carriers in the semiconductor are repelled from the oxide/semiconductor interface resulting in a space-charge layer. This is assuming that the applied bias is the same charge as the majority carriers in the semiconductor. The space-charge layer is populated of minority carriers and given the name majority-carrier depletion layer.[36]

The frequency of the field applied to the capacitor can also affect the trap layer in the semiconductor. Traps within the semiconductor material become filled with carriers being attracted to the dielectric/semiconductor interface. When the bias is released, the traps are emptied. If the frequency becomes too high, the traps do not have sufficient time to empty and form a charge layer. At low frequencies, this layer is almost non-existent. As the frequency is increased, however, this trap layer becomes thicker and adds to the total capacitance. Capacitance measurements must be made at extremely low frequencies, called quasi-static frequencies, to obtain the capacitance that is purely within the dielectric material. A more complete explanation of ideal and real capacitance-voltage measurements is given in Appendix 1.

2.1.3 The metal/insulator/semiconductor transistor

Modern chips are based on complementary pairs of metal oxide semiconductor (CMOS) transistors. This is one of most common devices found in logic and memory circuits. The gate region of the transistor determines the capabilities of the device. There are two types of MOSFET devices, depletion mode and enhancement mode. In the depletion mode device, the material type under the source, gate, and drain regions is the same. This device is in the "ON" state when there is no applied gate voltage. In the enhancement mode device, the material type under the gate is opposite to that under the source and drain. This device is in the "OFF" state when there is no applied gate voltage. Diagrammed in Figure 2.1 is a cross-section of a depletion mode MOSFET. Due to the relatively low p-type carrier concentration available for p-GaN, only n-type depletion mode devices were considered.

The n-MOSFET will be used to describe the operation of the gate in the transistor. For a p-MOSFET, the gate voltage is reversed. When there is a zero gate voltage, carriers are free to flow from the source to the drain in the MOSFET structure. The switch is "ON." As a negative voltage is applied to the gate contact, electrons under the gate dielectric are repelled (like charges repel) and a positive charge is induced in the semiconductor under the gate region. This positive charge hinders the ability for electrons to flow from the source region to the drain region. As the gate voltage is increased, more positive charges collect under the gate until the flow from source to drain is stopped. This voltage is called the pinch-off voltage, since it effectively pinches the channel shut. The transistor is now "OFF." As the current through the source-drain is increased, it requires more gate voltage to successfully pinch-off the carrier flow. Thus the maximum operating parameters of the device are determined by the amount of electric field that can be applied to the gate before dielectric breakdown occurs.

2.2 SiC Based Electronic Devices

The first SiC based device was a light emitting diode fabricated in 1907 by H.J. Round. The wide bandgap, high thermal stability, and the availability of SiC single crystal wafers make it an attractive material for fabrication of high power/high temperature electronic devices. There have been two major dielectric materials researched for SiC based devices, silicon oxide (SiO_x, E_g=9.0eV) and aluminum nitride (AlN, E_g=6.2eV). Silicon nitride (Si_3N_4) has been considered as a dielectric, but the bandgap (E_g=5eV) is small enough to allow for tunneling at the SiC/Si_3N_4 interface.

2.2.1 Silicon oxide on SiC

Silicon oxide is a very attractive choice for a dielectric material since it is the native oxide of SiC. The entire silicon (Si) industry today would not have developed so rapidly if it had not been for the dielectric properties of the native oxide. Silicon oxide has been well studied and the processing is well established. Several groups have researched SiO_x as a possible dielectric material for SiC. Several methods of creating SiO_x films have been investigated. Dry oxidation of 6H-SiC has given room temperature interface state densities of $2x10^{11}$ $eV^{-1}cm^{-2}$ and elevated temperature (300°C) interface state density of $8x10^{11}$ $eV^{-1}cm^{-2}$.[37] These values were calculated using the Terman method.[38] This dry oxidation was preformed at 1150°C for 7 hours using a flow of 0.5 sccm of O_2 to produce an oxide of 495 Å. This was carried out without any surface pretreatment to the SiC. Wet oxidation of SiC at 1150°C has shown an interface state density of $1.5x10^{11}$ $eV^{-1}cm^{-2}$.[39] The surface pretreatment of the SiC was shown to have profound effects on the interface state density. Following the oxidation, a 30 minute argon anneal at 1150°C allows for a fixed dielectric charge density of as low as $9x10^{11}$ $eV^{-1}cm^{-2}$. This same group has recently improved their technique and obtained an interface state density of $7x10^{10}$ $eV^{-1}cm^{-2}$ and fixed dielectric charge density of $5x10^{11}$ $eV^{-1}cm^{-2}$.[40] There are a few problems associated with the thermal oxidation of SiC. During the oxidation process, SiC is consumed. Consumption of SiC becomes a concern when dielectrics are needed over thin, heavily doped regions of the SiC surface. Also, SiC has two stable surfaces, silicon and carbon. Each of these surfaces has different oxidation properties which must be controlled to ensure a predictable oxide film.

Other methods for creating SiO_x involve the deposition of an oxide film. This method is desirable over the thermal oxidation process since none of the SiC surface is consumed in the process. Plasma-enhanced chemical vapor deposition (PECVD and low-pressure chemical vapor deposition (LPCVD) use precursors of silicon and oxygen in a reactor tube to deposit the silicon oxide.[41,42] Still other methods include: deposition of a silicon layer for oxidation[42], remote RF plasma deposition of silicon oxide[43], and jet vapor deposition (JVD) of silicon oxide[44]. It was found that the dielectrics produced from these techniques were not as useful as the thermal oxides. The lowest values of interface state density and fixed dielectric charge were produced by the wet oxidation technique used in reference 4. While these trap densities are low enough for successful devices, there are inherent problems with SiO_x as a dielectric material for wide bandgap semiconductors. First, the SiO_x is not as thermally stable as one would like for prolonged high temperature device operation. Add to that a difference in thermal expansion between SiC and SiO_x and the device lifetime at high temperature becomes very limited. Also, SiO_x has a dielectric constant (ε) of 3.9, which is significantly lower than that of SiC (ε=10). This will create a very large electric field in the dielectric, leading to further breakdown.

2.2.2 Aluminum nitride on SiC

Aluminum nitride has shown many promising attributes as a dielectric material for wide bandgap semiconductors. First, it has a dielectric constant (ε=8.5) comparable to the wide bandgap semiconductors. It also has high thermal and chemical stabilities. The thermal expansion is similar to that of SiC, allowing for less thermal stress at operating temperature. Aluminum nitride is closely latticed matched to SiC (1.0%

mismatch). There have been several groups who have researched AlN epitaxy on SiC.[42,45,46,47,48,49,50,51,52] The deposition techniques have been gas-source MBE, MOCVD, plasma-source MBE, pulsed laser deposition, and helium supersonic beam deposition. Aluminum nitride has been researched for use as seed layers for GaN growth, dielectric films, and capping layers for SiC high temperature anneals.

Film nucleation, orientation, and growth on different crystal faces and miscuts have led to high quality single crystal AlN films.[46,49,50] Single crystal films have been reported at growth temperatures as low as 500°C, and polycrystalline films as low as 400°C. Surface analysis has shown the single crystal AlN films are rougher than the polycrystalline films. This is due to the columnar type growth that is associated with AlN single crystal films. Single crystal AlN has been reported to be thermally stable at temperatures as high as 1500°C.[52] The AlN was chemically stable up to 1600°C, but the AlN capping layer cracked, buckled, and separated from the SiC substrate. Also, an amorphous intermediate layer of AlN forms between the single crystal AlN and the SiC substrate. Single crystal aluminum nitride as a dielectric has shown promising results. An interface state density of $1x10^{11}$ $eV^{-1}cm^{-2}$ has been reported.[47] Varying the microstructure has shown that a single crystal AlN dielectric is superior to a polycrystalline AlN dielectric. It has been theorized that the grain boundaries of the polycrystalline AlN cause shorting through the dielectric film.[51] Single crystal AlN has a critical thickness of 4.6nm on SiC with the 1.0% mismatch in the lattice. Threading dislocations forming on the silicon steps of the SiC surface have been shown to add to the shorting of the dielectric film.

2.3 GaN Based Electronic Devices

Gallium nitride research has resulted in long-lifetime, room temperature operation of photonic devices. These include LEDs that cover the visible spectrum, laser diodes in the blue and blue-green regime, and UV detectors. These devices are just recently reaching production level, with problems still to be solved in the fields of n-ohmic and p-ohmic contacts, p-type doping issues, Schottky contacts, and dielectric materials. Also, with the lack of availability of GaN substrates, research of epitaxial growth and substrate selection is still ongoing. From material and processing advances learned from the photonics research, high-power and high-temperature switches have been realized. Below are summarized some of the dielectric materials researched to date.

2.3.1 Silicon oxide on GaN

Silicon oxide deposited by plasma enhanced chemical vapor deposition (PECVD)[53,54,55] has been reported to give interface state densities on the order of low $1x10^{11}$ $eV^{-1}cm^{-2}$. Silicon oxide deposited by electron beam (EB) evaporation has shown interface state density of $5.3x10^{11}$ $eV^{-1}cm^{-2}$.[55] The EB evaporated SiO_x shows a silicon rich stoichiometry when compared to the PECVD SiO_x. Several of the problems identified with SiO_x on SiC also apply to the GaN devices.

2.3.2 Silicon nitride on GaN

Silicon nitride deposition by PECVD[55,56] reported an interface state density of $6.5x10^{11}$ $eV^{-1}cm^{-2}$. This value is reasonable for a first attempt. But when compared to GaN MESFETs, the Si_3N_4 MISFET was out preformed. Electrical measurements showed

the MISFET structure had a large flat band voltage shift (3.07 V) and a low breakdown voltage (1.5 MV/cm) of the dielectric. There was no microstructure analysis performed on the deposited Si_3N_4 films.

A unique dielectric structure of $SiO_2/Si_3N_4/SiO_2$ (ONO) was reported to have a breakdown field strength of 12.5 MV/cm for temperatures as high as 300°C.[57] The ONO structure was deposited by jet vapor deposition to a thickness of 10nm/20nm/10nm. This multilayer structure does allow for unique engineering of a dielectric, but multiple interfaces can lead to an extremely large number of interface state traps and increased processing.

2.3.3 Aluminum nitride on GaN

Aluminum nitride deposited by MBE and MOCVD has been used to create MISFET devices and insulated gate heterostructure field effect transistors (IG-HFET) devices.[58,59] The AlN MISFET structure grown at 400°C was polycrystalline. From x-ray reflectivity measurements, the AlN/GaN interface showed a roughness of 2.0nm. This may be due to the polycrystalline nature of the film or from intermixing of the AlN and GaN. The dielectric breakdown field was calculated to be 1.2 MV/cm. The AlN IG-HFET structure was grown at 990°C, forming a single crystal film of 4.0nm. This device operated in enhancement mode and had a pinch-off voltage of 0 V. Hexagonal aluminum nitride has a 2.4% lattice mismatch with hexagonal GaN on the (0001) plane. The 4.0nm film thickness is greater than the critical thickness allowed for elastic deformation. This leads to threading dislocations forming from plastic deformation. Single crystal AlN and polycrystalline AlN films suffer from defects and grain boundaries that cause shorting.

2.3.4 Gallium oxide on GaN

Gallium nitride forms a stable native oxide. This oxide has been considered as a dielectric material, like the native oxide of silicon. Thermal oxidation of the GaN surface has lead to some interesting research. Oxidation was performed in dry[60,61] and wet[62] atmospheres. Dry oxidation of GaN epilayers at temperatures below 900°C showed minimal oxidation. At temperatures above 900°C, a polycrystalline monoclinic Ga_2O_3 forms at a rate of 5.0nm/hr. This oxidation rate is too slow to be viable as a processing step. Wet oxidation of GaN also forms polycrystalline monoclinic Ga_2O_3, but at a rate of 50.0nm/hr at 900°C. From cross-sectional transmission electron microscopy, the interface between the oxide and the GaN is found to be non-uniform. Scanning electron microscopy shows that both films are rough and faceted. Electrical characterization of the oxide films shows the dry oxide dielectric has a breakdown field strength of 0.2 MV/cm and the wet oxide dielectric field strength of 0.05 to 0.1 MV/cm. Some limits to the thermal oxidation of GaN are that only one microstructure has been formed from this process and GaN is consumed in the process.

2.3.5 Gallium gadolinium oxide on GaN

Due to recent the success of gallium gadolinium oxide (GGG) as a dielectric in GaAs MOSFETs,[63,64,65,66,67,68] attention has turned toward this as a dielectric material for GaN. The GGG dielectric was deposited on a GaN epilayer by EB evaporation of a single crystal GGG source.[58] The substrate temperature was 550°C. Interface roughness was calculated to be 0.3nm from x-ray reflectivity. Metal oxide semiconductor (MOS) capacitors were formed and tested. A breakdown field of >12MV/cm was estimated. More recently, the thermal stability of the film and interface has been proven to

temperatures as high as 950°C[69] and the operation of a depletion mode MOSFET has been performed at temperatures up to 400°C[70]. The EB evaporated GGG stoichiometry is heavily dependant upon the substrate temperature as changes in temperature lead to changes in stoichiometry.[71] This limits the available microstructure obtainable within the stoichiometric limits of the GGG.

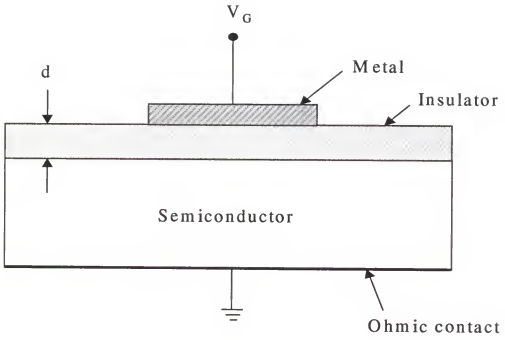


Figure 2.1 Illustration of a typical metal-insulator-semiconductor capacitor

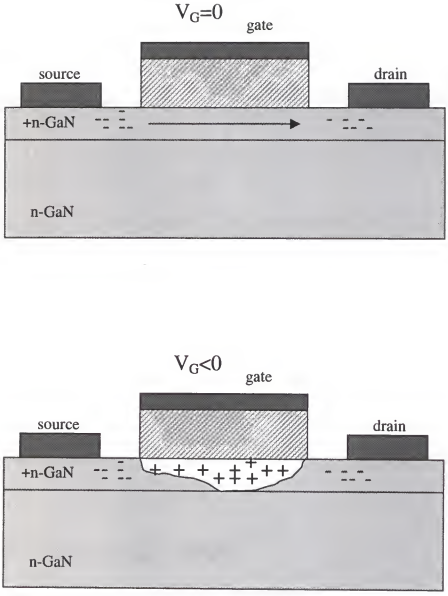


Figure 2.2 Cross-section illustration of a depletion mode n-MOSFET. In the top figure, the device is in the "ON" state with V_G=0. The bottom figure is the device in the "OFF" state with V_G<0, notice the conduction channel is pinched-off.

CHAPTER 3
EXPERIMENTAL APPROACH

3.1 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is the growth method employed in this work to produce the dielectric films. The dielectric materials were deposited in an ultra-high vacuum environment from the purest attainable elements. In MBE, the individual elements of the compound are provided to the growth surface independent of each other, allowing for a high degree of control over the stoichiometry of the dielectric material that conventional sputtering and electron beam evaporation do not allow. Also, MBE allows for precise control of the substrate temperature, which in turn, helps to control the microstructure of these materials. The growth rate is dependant upon the substrate temperature, the ratio of the elements, and also the rate at which the elements are supplied to the substrate.

In conventional MBE, beams of atomic or diatomic species are produced from special ovens called Knudsen cells, Figure 3.1. The purity of the atomic beam depends upon the vacuum level in the chamber and the purity of the starting material. The number of atoms emitted from the Knudsen cell is related to the temperature of the cell and the relative atomic mass of the material in the cell. This relation is determined by equation (3.1) where F is the flux of the Knudsen cell in atoms/cm^{2}s, p is the vapor

pressure in the cell in Torr, a is the orifice area in cm^2, d is the cell to substrate distance in cm, M is the atomic mass of the element in amu, and T is the temperature of the cell in Kelvin.

$$F = \frac{1.118 \times 10^{22} (p)(a)}{d^2 (MT)^{1/2}} \quad (3.1)$$

For the oxides, a Riber model 2300 MBE was modified to perform the growth. A sketch of this system can be seen in Figure 3.2. The main growth chamber was pumped with a cryopump allowing for a base pressure of 2×10^{-7} Torr. This modified MBE is equipped with a Reflection High-Energy Electron Diffraction (RHEED) system, described in section 3.2.1. This allows for the arrangement of the top few monolayers of atoms to be determined. This is extremely important in determining the atomic arrangement of the starting growth surface and in determining the structure of the film.

The oxygen source for the oxide growth was provided by a WaveMat model 610 ECR plasma source, Figure 3.3, operating at a frequency of 2.54 GHz and powers ranging from 100 to 200 watts. Oxygen is supplied through a leak valve using a 99.995% oxygen source. The microwave energy is guided into the source chamber and coupled into the oxygen molecule electron cloud. A series of permanent magnets around the source chamber create a magnetic field which accelerates the electron motion into helical paths that collide and ionize the source gas molecules. This creates a dense plasma in the source chamber. The plasma contains the atomic species for growth, as well as ionic and molecular species.

The aluminum nitride was grown in a modified Varian Gen II MBE system, as in Figure 3.4. This ultra-high vacuum system is equipped with both solid and gaseous

sources, making it a very flexible research tool. The nitrogen source is a remote radio frequency (RF) plasma source operating at 13.9MHz. The nitrogen is supplied as 99.999% pure gas. The RF plasma breaks down the neutral diatomic nitrogen molecule into more reactive atomic and ionic species. This is preferred over the more common chemical vapor deposition (CVD) growth that uses ammonia as a nitrogen source. The process of using ammonia as a nitrogen source requires much higher substrate temperatures to decompose the ammonia molecule, and would limit the temperature regimes of this research.

The aluminum was supplied from a liquid compound, dimethylethylamine alane, supplied in a bubbler, using high purity helium as a carrier gas. Figure 3.5 shows a diagram of the operation of a bubbler. The use of metal-organic sources has many benefits, the largest one being the sources are located outside of the ultra-high vacuum chamber so they can be changed without venting the vacuum chamber. However, there are disadvantages as well. The two of most concern are the carbon contamination associated with the decomposition of the metal-organic species and the minimum source temperature required for sufficient breakdown of the metal-organic species. These properties set a low temperature limit for the aluminum nitride growth.

The substrate temperature was determined by a back side thermocouple in close proximity with the substrate holder. The substrate thermocouple was calibrated by using the melting points of gallium antimonide, GaSb, (707°C) and indium antimonide, InSb, (525°C). Pieces of GaSb and InSb were heated in the growth position with a nitrogen plasma impinging on the surface. This reduced the chance for loss of the group V, Sb, during the heating, which would result in an incorrect melting temperature.

3.1.1 Substrate preparation

Prior to any epitaxial growth, the substrates received an ex-situ and an in-situ surface treatment to remove any contamination and the native oxide. The surface of the semiconductor must be as clean and planar as possible to ensure high quality dielectric film deposition. Surface contamination leads to impurities at the dielectric/semiconductor interface, which ultimately result in creating interface traps, as described in section 2.1.2. The substrates were visually inspected as well as scanned using atomic force microscopy (AFM), described in section 3.2.4. This gave a reference for surface roughness to compare against the final growth product. Substrates used in this work are silicon (Si), gallium nitride (GaN), and silicon carbide (SiC).

Silicon. Although silicon is not considered a wide bandgap semiconductor, all of the initial experiments were carried out on Si single crystal substrates oriented in the <001> direction. This was used due to the wide availability of Si substrates and their low cost. The data gathered from the Si substrates is used to calibrate the growth rate and composition of the dielectric films. The microstructure of the dielectric films grown on Si will be different from that on the GaN and the SiC since the surface atomic spacing and the crystal structure of the substrate are different.

Silicon wafers received an ex-situ treatment of a 30 second wet etch in a buffered oxide etch solution, consisting of 6 parts ammonium fluoride and 1 part hydrofluoric acid, rinsed in deionized water (DI), and dried under nitrogen gas. This treatment results in a smooth surface with a surface roughness root mean square (RMS) value of 0.08nm, as seen in AFM. This surface is oxide free and is stable for a period of up to 1 hour.

Gallium nitride. Since gallium nitride wafer substrates are not currently available, gallium nitride grown on sapphire wafers oriented <0001> were used. These will be referred to throughout this work as GaN substrates. Two different types of growth of the GaN substrates were employed in this work, MBE and metal-organic chemical vapor deposition (MOCVD). The MBE GaN substrates were provided by SVT Associates and the MOCVD substrates provided by Epitronics. From AFM, there is a large difference in surface roughness between these samples. The MOCVD substrates are 1-3nm RMS roughness and the MBE substrates are ~6nm RMS roughness, as shown in Figure 3.6.

The GaN substrates received an ex-situ treatment consisting of a 3 minute etch in (1:1) hydrochloric acid:water, DI rinse, nitrogen dry. This was used to remove any organic residue from the surface. Then a 25 minute exposure to ozone produced by an ultraviolet lamp in a UVO Cleaner model 42-220 was used to oxidize the carbon on the surface and create a thin native oxide. Next, the substrates received another etch in buffered oxide etch, described for silicon, to remove the native oxide. This can be proven by observing the reflection high energy electron diffraction (RHEED) pattern produced from the surface, described in section 3.2.1. The RHEED pattern produced by the native oxide is more diffuse than the pattern produced by the buffered oxide etched surface, as seen in Figure 3.7.

The GaN substrates were then mounted to molybdenum blocks using indium solder, then loaded into the load/lock of the MBE. Room temperature RHEED measurements showed a reasonably clean (1x1) surface, Figure 3.7. Two different crystal directions are observed in RHEED to create a more complete surface understanding. Here, the <1-100> and the <11-20> directions are observed. An in-situ

thermal treatment was employed to further remove any oxide or contamination left on the surface. The substrates were heated to 700°C in vacuum and no overpressure of nitrogen was used. The RHEED patterns recorded at this temperature indicate a sharp (1x3) pattern, seen in Figure 3.8.

Silicon carbide. The 6H silicon carbide used in this work was provided by Dr. Carl-Mikael Zetterling of Sweden's KTH, Royal Institute of Technology. The as received SiC substrates have a smooth surface morphology as seen in scanning electron microscopy images and an AFM surface roughness RMS of about 0.1nm, Figure 3.9. This was found for both n-type and p-type substrates. From visible inspection, however, these substrates did suffer from a high density of pits on the surface. This is typical of many SiC substrates.

The SiC substrates received an ex-situ treatment of a 3 minute etch in a buffered oxide etch solution, as used in the Si and GaN substrates. The substrates were rinsed in deionized water and dried in nitrogen. They were then mounted to molybdenum blocks using indium solder and loaded into the load/lock.

3.1.2 Aluminum nitride growth

As stated earlier, the initial growths were performed on Si substrates. Substrate temperatures were 325°C, 375°C, and 425°C. These temperatures were chosen since the desired AlN microstructure was amorphous rather than polycrystalline. Temperatures below 325°C were assumed to be too low for sufficient decomposition of the metal-organic precursor. The nitrogen source was set to a forward power of 400 watts and the flows ranged from 2 sccm to 8 sccm. The aluminum source was held to a bubbler

temperature of 9.1°C, a bubbler pressure of 7.0 Torr, and a He flow of 10.0 sccm. In all cases, the rotation was kept at 15 rpm.

3.1.3 Gallium oxide growth

The gallium oxide films were grown in the modified RIBER 2300 MBE. The gallium was 99.9999% pure and Knudsen cell temperatures ranged from 860°C to 1110°C. The substrate temperature was varied from 300°C to 625°C. The WaveMat 610 ECR plasma source was set to 200 watts forward power and an oxygen pressure that varied from $3x10^{-5}$ Torr to $1x10^{-4}$ Torr.

The Riber 2300 MBE was also equipped with a custom electron beam (e-beam) evaporation source, produced by SVT Associates, Figure 3.10. Unlike in conventional electron beam evaporation cells, in the custom SVT e-beam cell electrons are not focused directly to the source material as a beam, but are rather drawn to a conductive metal crucible by use of a positive bias up to 3 kV. This causes the crucible to be heated, like a conventional effusion cell. Temperatures of over 2000°C are said to be obtainable. The temperature of the crucible is regulated by the power in the electron filament and the bias on the crucible. A charge of 99.9% pure gallium oxide is placed into the conductive crucible. The filament power was set to max, about 80 watts, and the crucible bias varied from 1kV to 2.5 kV. Substrate temperature was kept constant at 550°C.

3.1.4 Gadolinium oxide growth

The gadolinium oxide samples were grown in the same Riber 2300 MBE as the gallium oxide. The gadolinium metal, 99.99% pure vacuum solidified, was used and the cell temperature ranged from 1175°C to 1270°C. These cell temperatures are at the upper

limit of the cell operating range. The ECR plasma power was kept at 200 watts forward power and the pressures ranged from $1x10^{-4}$ Torr to $5x10^{-4}$ Torr. Substrate temperatures ranged from 300°C to 650°C. Attempts were made to use the SVT e-beam as a source for gadolinium metal, since the Knudsen cells were pushed to their limits. The crucible was removed from the cell and a ¼ inch rod of gadolinium was put in its place. Bias can be applied to the rod allowing the e-beam cell to behave more like a standard e-beam cell. However, when the oxygen for the plasma was leaked into the chamber, the e-beam power rose sharply and the beam shut off. The oxidation of the hot filament reduced the electron emission from the filament, and the feedback loop of the power supply would ask for more power. This would continue until the power supply would go into overload.

The e-beam cell with crucible was used with a charge of 99.9% gadolinium oxide. Similar bias and powers were used as in the gallium oxide deposition. The substrate temperature was varied from 300°C to 600°C when using the e-beam source with the gadolinium oxide charge.

3.1.5 Magnesium oxide growth

The magnesium oxide samples were grown from 99.99% pure magnesium and Knudsen cell temperatures ranged from 350°C to 400°C. The oxygen plasma was constant at 200 watts forward power and $1x10^{-4}$ Torr pressure. Substrate temperatures were varied from 600°C to 650°C. Due to the extremely high melting temperature of magnesium oxide (2850°C), evaporation of magnesium oxide from the custom e-beam source was not attempted.

3.2 Materials Characterization

Once the films were grown, they were heavily characterized. Emphasis of the research was placed on, but not limited to, the microstructure and the stoichiometry of the epitaxial films and how these properties relate to the electrical properties and thermal stability of the dielectric materials. The dielectric films were annealed to temperatures as high as 1100°C by a rapid thermal anneal (RTA) process to determine the thermal stability of the films.

3.2.1 Reflection high energy electron diffraction

Both modified MBE systems are equipped with reflection high-energy electron diffraction (RHEED) systems. A RHEED system consists of an electron gun, typically 5 to 30 kV, and a phosphorescent screen. The electrons from a filament are collimated, accelerated, and reflected off the surface of the sample. A diffraction pattern is seen on the phosphorous screen. From this diffraction pattern, single crystal, polycrystalline, and amorphous films can be delineated. This technique was used to determine the starting substrate surface quality and the quality of the films grown while in the ultra-high vacuum system. A detailed explanation of the RHEED apparatus and characterization technique is given in Appendix 2. Also, the method of growth initiation, which has an enormous impact on the overall film quality, can be determined from RHEED.

RHEED reflections are created by diffraction from the surface atoms of the substrate. The incoming electron beam has an incident angle of 1 to 2 degrees. Diffraction occurs only along certain crystal directions in a single crystal sample. From the type of pattern, intensity, and spacing between diffraction events, a 2-dimensional

map of the surface can be created. It is this map that will help determine the starting substrate surface as well as the film grown. Polycrystalline surfaces show a ringed pattern and amorphous surfaces show almost no pattern at all, Figure 3.11. The diffraction is so surface sensitive, fractions of monolayers can be determined. This technique was employed in this work to determine the substrate surface preparation, growth initiation, and epitaxial film structure.

3.2.2 Transmission electron microscopy

One of the most powerful microstructural analysis techniques available is transmission electron microscopy (TEM). From TEM, not only can the microstructure of an epitaxial film be determined, but detailed analysis of defects in the film, atomic imaging of the interface, and accurate calculation of lattice spacing is determined. One of the major drawbacks of TEM is the sample preparation required to obtain the images. The sample must be cut, polished, and thinned to electron transparency (~100nm) via ion beam thinning. A complete description of the sample preparation is given in Appendix 3. This is especially difficult for the nitride and carbide materials due to their hardness. A JEOL 200CX operating at 200keV was used for film analysis and a JEOL 4000FX operating at 400keV was used for high-resolution analysis of the interfaces.[72]

3.2.3 High resolution x-ray diffraction

Another structural analysis technique is x-ray diffraction (XRD). This technique has virtually no sample preparation when compared to TEM. X-rays are diffracted off of the sample to produce characteristic peaks of the atomic planes in the sample. The full width at half maximum (FWHM) of these characteristic peaks is used to determine the

crystalline quality of the films. Powder x-ray diffraction can be used if the samples are polycrystalline or polycrystalline/amorphous, however, this was not employed in this research. X-ray reflectivity from the air/film interface and the film/substrate interface help to determine the roughness of these interfaces and the film thickness. The available x-ray system is a Phillips MPD 1880/HR with a 5 crystal analyzer. The x-ray source is Kα-Cu. Figure 3.12 shows an illustration of the sample geometry for x-ray diffraction. Samples were scanned measuring ω-2θ with the GaN peak optimized. From the x-ray scan, the 2θ peak positions are obtained and through Bragg's Law, equation 3.2, the d-spacing between the corresponding planes are calculated.

$$\lambda=2d\sin\theta \qquad (3.2)$$

Here, λ is the wavelength of the incident x-ray, d is the spacing between the planes and θ is the measured peak position. The d-spacings are compared to known values of the material to determine crystal orientation.[73]

3.2.4 Atomic force microscopy

The surfaces of the grown films were characterized using atomic force microscopy (AFM) to give a quantitative analysis. Tapping mode AFM was used to obtain a root mean square (RMS) roughness of the surface. In tapping mode, the tip of a stylus, made from Si_3N_4, is brought into close proximity of the surface, close enough to be deflected by the Van der Waal forces of the surface atoms. A laser is reflected off the AFM tip and collected into a photodiode, Figure 3.13. The intensity of the reflected light is read as a height. The tip is rastered across the surface and each point is read as a

height, creating a 3-dimensional map of the surface. From this 3-dimensional map, a surface roughness is calculated and from this a RMS roughness. This is very useful in characterizing the starting substrate, the dielectric film, and the effects of the various processing steps. The sensitivity of the AFM apparatus is dependant, among other things, on the sharpness of the tip and the sensitivity of the deflection. The tapping mode tip used here has a tip radius of 5nm and the deflection sensitivity is about 0.01nm. This makes the tapping mode extremely sensitive to surface roughness. An alternate mode of operation is contact mode. However, the tip radius of the contact tip is about 20nm, which greatly reduces the resolution. The AFM used in this study was a Digital Instruments Nanoscope III.

3.2.5 Scanning electron microscopy

The surfaces of the samples were characterized on the macro level by using secondary electron microscopy (SEM). The SEM used in this research is a JEOL 6400. This technique gives a qualitative analysis of the surface, indicating the overall surface morphology of the film. This is important for future processes in fabricating capacitors and MOS(MIS)FETs, since device processing requires annealing, etching, and metal deposition, all of which are sensitive to surface morphology. Although the SEM does not give a quantitative result like the AFM, it is useful to examine grossly rough surfaces that the AFM is unable to resolve.

In the SEM, an electron beam is accelerated through a high voltage field of 5kV to 30kV, toward the sample. The electrons strike the surface and penetrate to a certain depth, that is governed by the amount of acceleration from the field and the atomic number, Z, of the elements in the surface. The higher the Z value, the more dense the

surface and therefore the less penetration. A cross-section of this penetration and interaction with the sample is seen in Figure 3.14. Notice that at different levels in the material, different interactions take place. One of these interactions is the creation and release of secondary electrons from the surface. These secondary electrons are collected and converted into an image on a CRT. Figure 3.15 shows a simplified diagram of the workings of a scanning electron microscope.

3.2.6 Auger electron spectroscopy

Auger electron spectroscopy (AES) was used to determine qualitatively the elements present in the grown dielectrics. As seen in Figure 3.14, Auger electrons are also emitted from the sample during the electron/sample interaction. An incident electron strikes an inner shell electron of an atom and ejects that electron. An upper level electron fills the void and energy is given off in the form of an Auger electron. The Auger electron is specific in energy to the element it came from and is thus a characteristic electron to that element. The Auger electrons are collected and an elemental analysis of the surface is obtained. The AES technique can detect elements down to the alloy level (~1%) within the top 1.0nm of the surface. Auger electrons are produced throughout the interaction volume of the incident electrons, however, due to their low energies, only those produced near or at the surface can escape. From the ratio of the peak heights from each element and published sensitivity factors, an approximate ratio of elements can be determined. From this ratio, the approximate formula can be obtained. A Perkin Elmer 660 AES was used for these measurements. This system is also equipped with an ion gun for creating depth profile auger electron spectra. From this, changes in the element ratios perpendicular to the interface, and the interface itself, can be studied. This will help in

determining if the substrate preparation is sufficient to remove native oxides and contamination. Also, approximate film thickness can be determined from known standards.

3.2.7 Current-Voltage measurements

Current-voltage measurements were made using a Hewlett Packard Model 4145. In these measurements, the current is set to an upper and lower limit, typically 5μA to 10μA and the voltage is swept from negative to positive. The voltage range is increased until the forward and reverse breakdowns are reached, Figure 3.16. The current limit is then set to 1mA and the voltage is measured again. The voltage at 1mA is divided by the dielectric thickness and the breakdown field strength is obtained. This is one parameter used in defining the quality of the dielectric film. This will help to determine the breakdown field strength of the dielectric at elevated temperatures. A low breakdown field indicates an inherent weakness in the dielectric. There is a heated stage with the current-voltage measurement apparatus with a maximum temperature for the testing of 300°C. This was employed to study the dependence of temperature with the breakdown of the dielectric.

Ohmic contacts were made to the silicon substrates using a Pt/Au (300Å/1000Å) bilayer structure deposited using electron beam evaporation. Ohmic contacts made to the gallium nitride and silicon carbide were made using a multilayer structure of Ti/Al/Pt/Au. The contacts on the GaN and SiC were annealed for 30 seconds at a temperature of 450°C in a nitrogen ambiant. Contacts on the dielectric were Pt/Au and were deposited through a shadow mask with varying contact size. The most commonly used contact size was 300μm and 400μm.

3.2.8 Capacitance-Voltage measurements

Capacitance-voltage measurements were made using a Hewlett Packard Model 4284. Here a bias (2 to 20 volts) is applied across the capacitor and cycled at a selected frequency, typically 100Hz to 1Mhz, and the resulting capacitance is recorded. A quasi-static measurement was not performed due to insufficient electrical isolation of the apparatus. From the capacitance-voltage plots, the flat band voltage shift, dielectric constant, and interface state density can be calculated. Calculating the carrier concentration of the substrate from the data obtained can test the accuracy of these measurements. This carrier concentration should match the quoted value from the manufacturer.

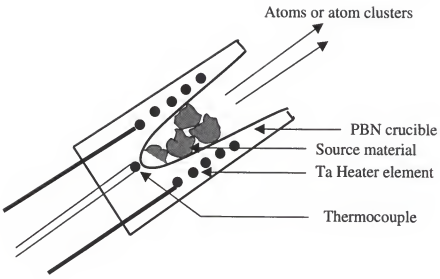


Figure 3.1 Illustration of a typical Knudsen effusion oven.

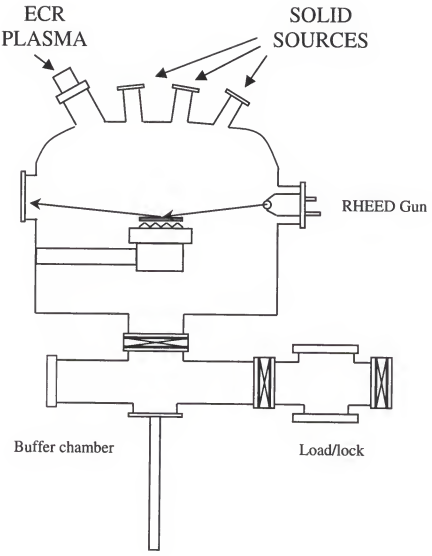


Figure 3.2 Illustration of Riber MBE used for oxide growth

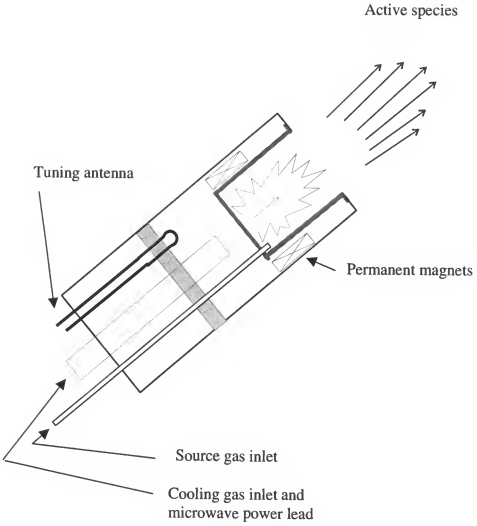


Figure 3.3 An illustration of the WaveMat 610 ECR plasma head.

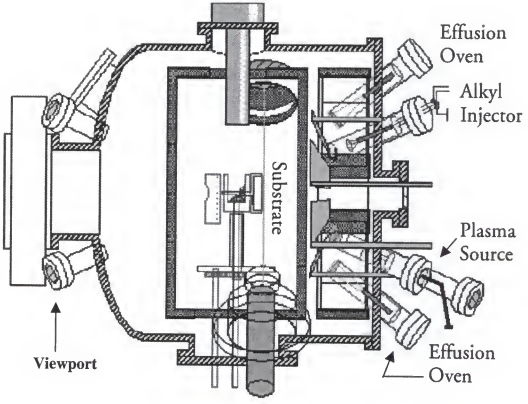


Figure 3.4 Illustration of the Varian Metal-Organic MBE used in the aluminum nitride growth experiments (after van der Wagt 1996). Only the growth chamber is shown.

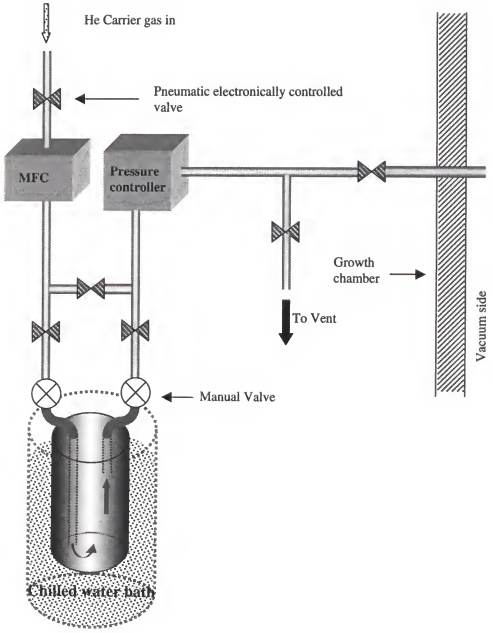


Figure 3.5 Illustration of a metal-organic bubbler and flow system used in the MOMBE growth method.

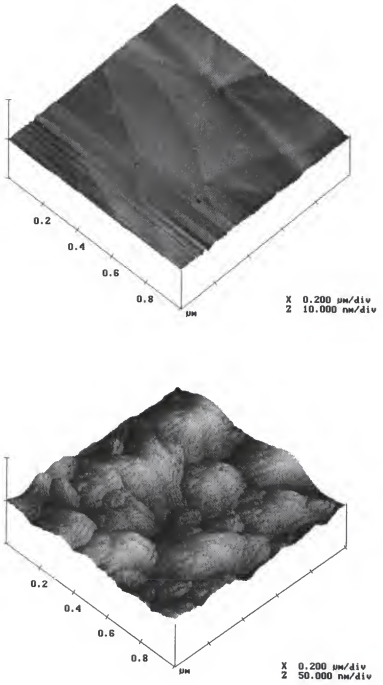
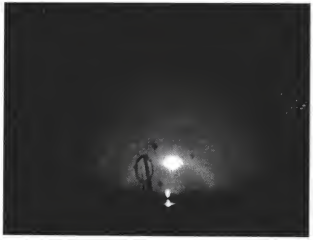
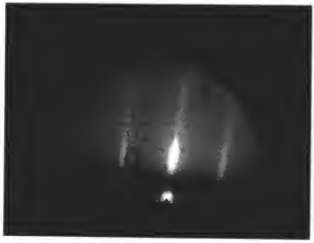


Figure 3.6 AFM images of as received MOCVD GaN (from Epitronics), top, and as received MBE GaN (from SVT).



(a)



(b)

Figure 3.7 RHEED images showing (a) the UV-ozone treated surface of MOCVD grown GaN and (b) the buffered oxide etched UV-ozone surface of GaN.

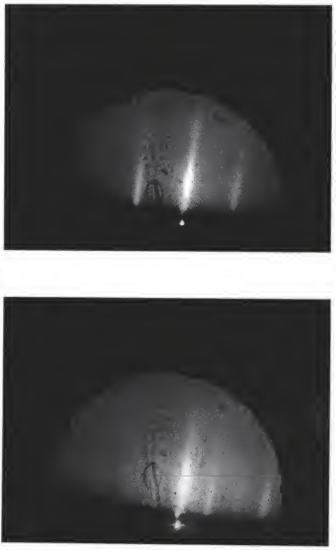


Figure 3.8 RHEED photos indicating a (1x3) pattern. The top photo is along the <11-20> crystal direction and the bottom photo is along the <1-100> crystal direction.

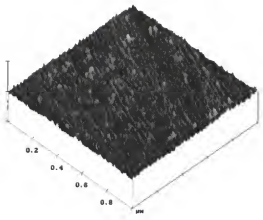


Figure 3.9 An AFM image (top) and a SEM image of as received n-SiC from Dr. Carl-Mikael Zetterling. The AFM scan area is $1\mu m^2$ with a surface roughness of 1.0nm. SEM bar length is $5\mu m$.

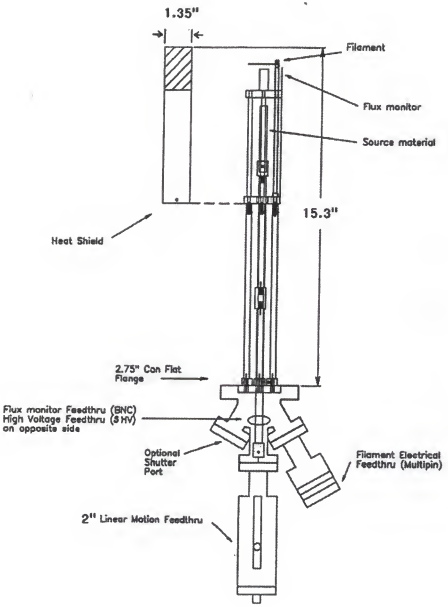
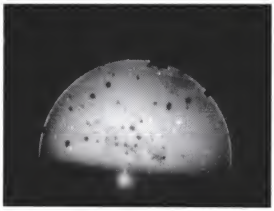
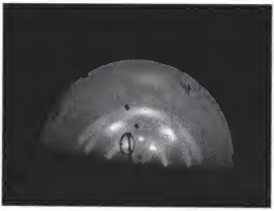


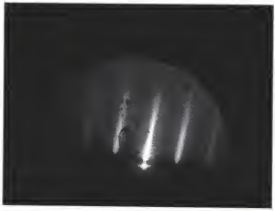
Figure 3.10 Illustration of the compact SVT electron beam source. The crucible replaces the rod source, just below the filament.



a



b



c

Figure 3.11 RHEED photos showing (a) an amorphous diffraction pattern, (b) a polycrystalline diffraction pattern, and (c) a single crystal diffraction pattern.

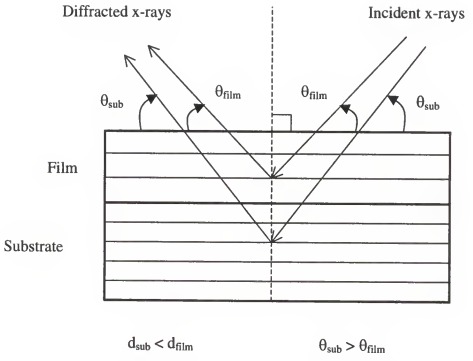


Figure 3.12 Illustration of the relation between the lattice parameter and Bragg angle for film and substrate.

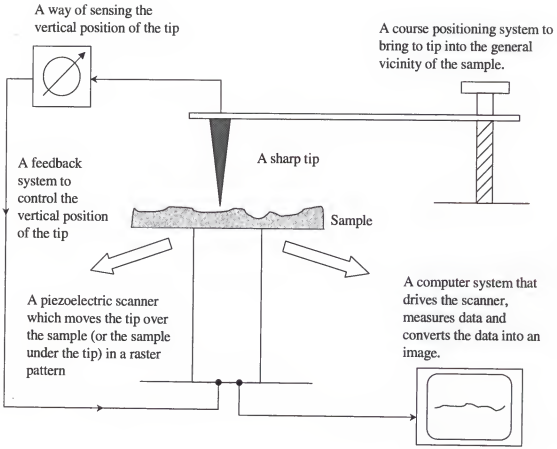


Figure 3.13 A schematic of the atomic force microscope (after K.K. Harris 2000)

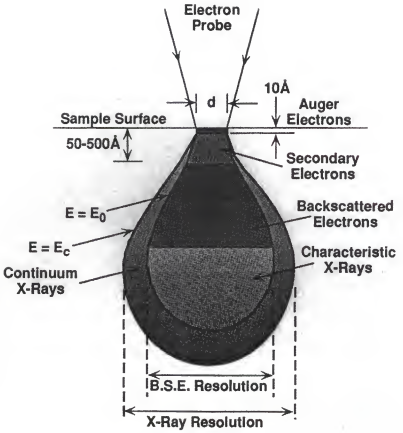


Figure 3.14 An illustration of the penetration depth and interaction of an electron beam in a material. Notice that Auger only escape the top 1.0nm (after Goldstein).

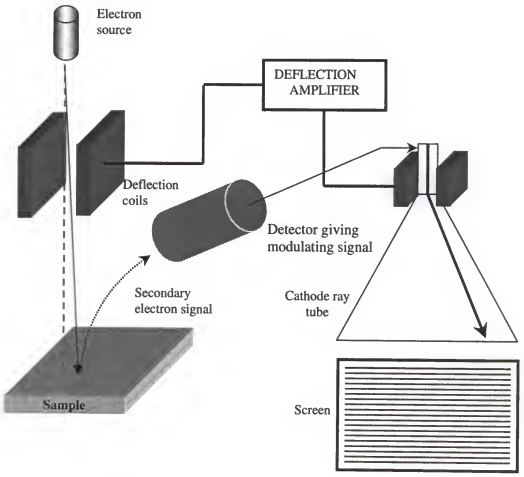


Figure 3.15 Illustration of SEM operation. Electron beam is rastered over the sample producing secondary electrons (after S.M. Donovan 1999).

CHAPTER 4
RESULTS AND DISCUSSION: Aluminum Nitride

Aluminum nitride has the same crystal structure as GaN with a lattice mismatch of 2.5%. The lattice mismatch between single crystal AlN and 6H-SiC is about 0.9%. Single crystal aluminum nitride can be grown on GaN at temperatures as low as 425°C using the growth method described in section 3.1.2. However, the single crystal AlN is plagued with a high density of defects that increase the density of fixed dielectric charge and interface states. To improve the electrical quality of the dielectric, the defect density must be reduced.

Aluminum nitride was initially grown on silicon (001) substrates at 425°C, 375°C and 325°C. The change in defect density and the change in growth rate was determined from cross-section TEM, as seen in Figure 4.1. Silicon has a cubic crystal structure therefore the single crystal AlN was not achieved at the 425°C substrate temperature. Rather a large grain polycrystalline structure was obtained as seen in Figure 4.1(a). The growth rates were 8.5 Å/min, 17 Å/min and 20 Å/min for the substrate temperature of 325 °C, 375 °C, and 425 °C, respectively. The structure of the aluminum nitride became slightly amorphous at 375°C and more amorphous at 325°C (Figure 4.1(b)). High-resolution TEM showed the 325°C growth temperature produced a Si/AlN interface that contained both amorphous and crystalline AlN, as seen in Figure 4.2. The amount of amorphous material in the film grown at 325°C was estimated to be ~ 30%. AES analysis

of the 325°C and 425°C samples showed that the AlN/Si interfaces are relatively clean and abrupt as seen in Figure 4.3. The depth profile results also demonstrated that the low growth temperature does not introduce carbon and/or oxygen contamination during the growth. This was a concern since the aluminum source material was a metal-organic and required a minimum substrate temperature to decompose. Tapping mode AFM analysis of as-grown samples showed that the root mean square (RMS) roughness of all of the three growth temperatures was less than 1 Å. The AFM image of AlN on Si is shown in Figure 4.4, and indicates that the surface morphology is independent of the growth temperature and structure. Included is an SEM image taken at 10,000x that showed no gross surface features, in agreement with the AFM images.

Capacitors were fabricated from these samples for electrical measurements. Current-voltage measurements of these samples showed that, on silicon, the dielectric produced breakdown field strengths of 2.9 MV/cm and 3.1 MV/cm for 325°C and 425°C grown samples, respectively (Figure 4.5). This showed that the reduction in growth temperature and change in structure did not greatly affect the breakdown field strength. Capacitance-voltage measurement of the AlN on Si showed that there was, however, a large difference between the samples (Figure 4.6). The measured flat band voltage shift for the as-grown samples was 3.8 V and 12.3 V for growth temperatures of 325°C and 425°C, respectively. The flatband voltage shifts were obtained from the capacitance-voltage plots. The method for obtaining the voltage shift values is discussed in APPENDIX 1. The large shift in flat band voltage between the two samples indicated that the fixed dielectric charge of the AlN was considerably reduced by the reduction in the growth temperature. The reduction in dielectric traps is assumed to be related to the

reduction of dangling bonds located in the grain boundaries. The amorphous material between the grains of the AlN can satisfy more bonds than an adjacent crystal. There was also a change in the slope of the capacitance-voltage plot. The 325°C grown sample showed a steeper slope than the 425°C grown sample. This indicated that the 325°C grown sample had a reduced interface trap density. From the high-resolution TEM image (Figure 4.2) the interface between the silicon and the aluminum nitride was a mixed amorphous/crystalline. If the traps were located in the grain boundaries, reducing the grain boundaries between the dielectric and substrate would reduce the interface state traps, as indicated by the capacitance-voltage plots. This reinforced the theory that the interface between the crystals was the source for the charge traps.

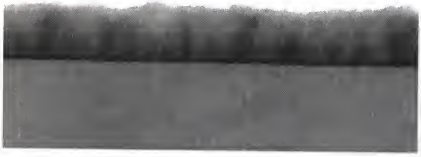
The as-grown samples received a 400°C annealing under forming gas (N_2H_2). The flat band voltage shift was reduced to 2.35 V and 11.7 V for the growth temperature of 325°C and 425°C, respectively. The 325°C grown sample showed a reduction in flat band voltage shift of 38%, while the 425°C sample was only reduced 5%. This indicated that the traps in the grain boundaries are more thermally stable and thus more difficult to reduce their density. The sample grown at 325°C received an 840°C anneal under forming gas and a nitrogen gas ambient and showed a flat band voltage shift value of 2.12 V, and 1.15 V, respectively. Table 4.1 summarizes the flat band voltage shift values of the samples. Atomic force microscopy images showed that the 400°C annealing treatment did not greatly increase the surface RMS roughness of the 325°C grown AlN (Figure 4.7 a and b). However, the 425°C grown AlN showed a large increase in surface RMS roughness after the anneal (Figure 4.7 c and d).

Table 4.1

T_g (°C)	as-grown	Forming Gas 400 °C	840 °C	N_2 gas 840 °C
325	3.8 V	2.35 V	2.12 V	1.15 V
425	12.3 V	11.7 V	—	—

The 325°C aluminum nitride was also grown on p-SiC. The as-grown p-SiC showed a surface RMS roughness of 0.1 nm, as seen in Figure 4.8. The dielectric thickness was about 170 Å. Capacitors were fabricated on this sample for electrical measurements. Current-voltage measurements on this sample showed the as-grown sample had a room temperature breakdown field strength of 6.8 MV/cm at 16 mA/cm^2 (Figure 4.9). At elevated temperatures, the breakdown field decreased to 3.9 MV/cm at 100°C, 2.9 MV/cm at 200°C, and 1.3 MV/cm at 300°C. The room temperature value was recovered after the sample cooled. This showed that the dielectric and the dielectric/semiconductor interface was not affected by the 300°C measurements. Capacitance-voltage measurements at room temperature showed the as-grown sample had a flat band voltage shift of –1.25 V (Figure 4.10). Again measurements were made at elevated temperatures. No shift in the flat band voltage was measured at the elevated temperatures. A decrease in the maximum capacitance was observed at the higher temperatures, but this too was recovered as the sample cooled.

(a) d = 400Å



(b) d = 163Å

Figure 4.1 Cross-section TEM of AlN on Si grown at (a) 425°C and (b) 325°C.

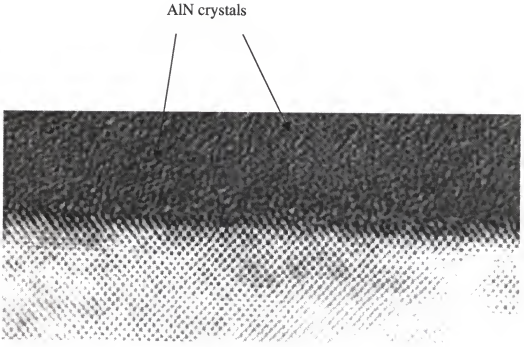


Figure 4.2 High resolution TEM of AlN on Si grown at 325°C. The film is on top and the substrate is on bottom. Arrows indicate AlN crystals in the amorphous AlN film.

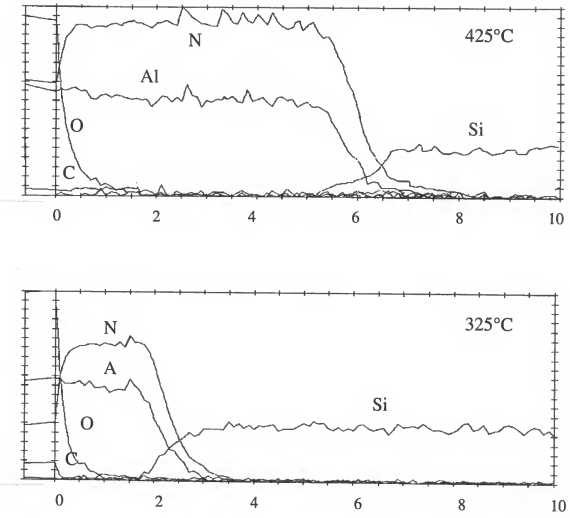
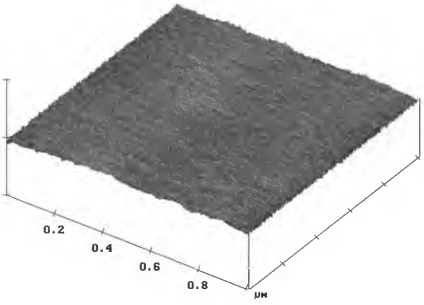


Figure 4.3 AES analyses of AlN on Si; (a) T_g = 425 °C, and (b) T_g = 325 °C for 20 minutes growth time.



(a)

(b)

Figure 4.4 Images of (a) AFM image of AlN grown on Si at 325°C and (b) SEM at 10,000x (bar length is 5 μm). The surface RMS roughness is about 0.1 nm.

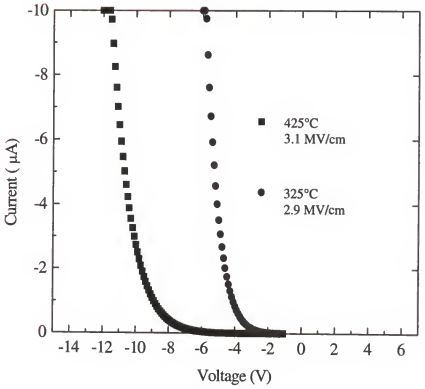


Figure 4.5 Current-voltage plots for AlN on p-Si grown at 325°C and 425°C.

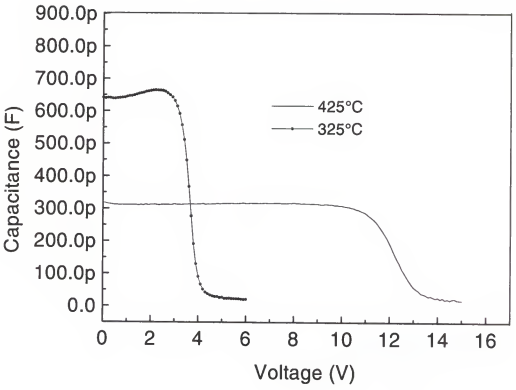
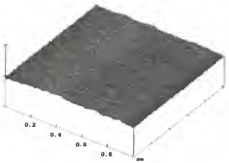
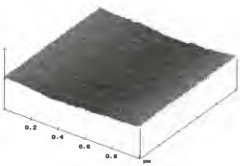


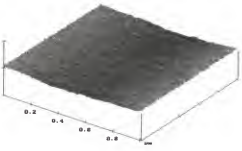
Figure 4.6 Capacitance-voltage plot of AlN on p-Si grown at 325°C and 425°C.



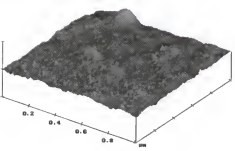
(a)



(b)



(c)



(d)

Figure 4.7 AFM images of 325°C grown AlN (a) as-grown and (b) annealed at 400°C and 425°C grown AlN (c) as-grown and (d) annealed at 400°C. Surface RMS roughness values are (a) 0.1 nm, (b) 0.2 nm, (c) 0.1 nm, and (d) 0.8 nm.

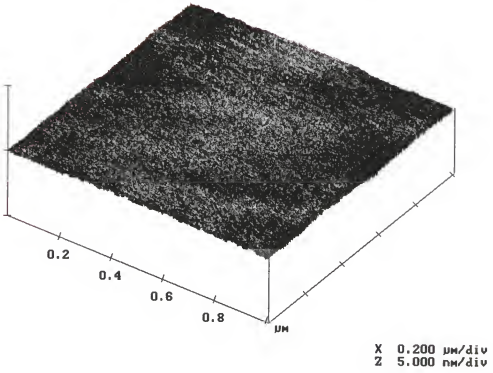


Figure 4.8 AFM image of AlN on p-SiC grown at 325°C. The RMS roughness is about 0.1 nm.

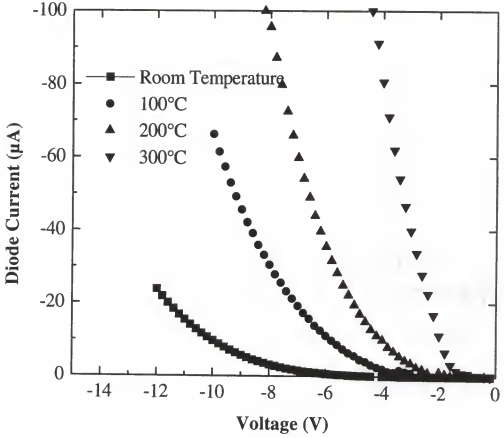


Figure 4.9 Current-voltage plot of AlN on p-SiC grown at 325°C. Included are measurements taken at elevated temperatures.

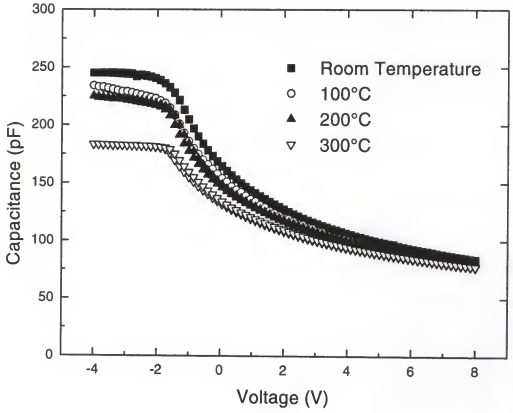


Figure 4.10 Capacitance-voltage plot of AlN on p-SiC grown at 325°C. Included are measurements taken at elevated temperatures.

CHAPTER 5
RESULTS AND DISCUSSION: Gallium Oxide

Gallium oxide was selected as a possible dielectric material since it is the native oxide of gallium nitride. Gallium oxide has three stable crystal structures, monoclinic, cubic and hexagonal. The hexagonal Ga_2O_3 structure has symmetry similar to GaN and SiC. However, the mismatch of the hexagonal with the gallium nitride is over 56%. Gallium oxide also exists in the GaO_2 chemical structure that has an amorphous structure and a lower melting point of 933K. This makes growing the gallium oxide difficult.

The gallium oxide growth was described in section 3.13. Initial experiments were performed on Si substrates. A substrate temperature of 540°C and an oxygen plasma pressure of $5x10^{-5}$ Torr were fixed and the gallium effusion cell temperature was varied from 1050° to 1110°C. For all samples grown at these conditions, the Ga_2O_3 films were weakly bonded to the surface and could easily be removed by scratching the surface with tweezers or a toothpick. The surface appeared to be porous and extremely rough to the naked eye. These films were thought to be polycrystalline with very poor morphology. An SEM image of this surface is shown in Figure 5.1. The oxygen to gallium ratio was determined from AES surface scans. The deposition rate and the oxygen to gallium ratios are plotted verses the gallium effusion cell temperature in Figure 5.2. As the cell temperature is decreased, both the deposition rate and the gallium incorporation rate decreased. However, the oxygen to gallium ratio is well above that measured from a

stable lump of Ga_2O_3. The surface roughness decreased and film bonding increased for these samples. However, these films did not last the masking and etching to create the capacitors to test the electrical results. Due to these results, the samples were not characterized further.

The substrate temperature was reduced to 400°C and the experiment was repeated. The gallium effusion cell temperature was varied from 1082° to 883°C. These results are plotted in Figure 5.3, along with results from the 540°C substrate temperature growths. At the 400°C substrate temperature, the oxygen to gallium ratio is more stable over a large range of Ga effusion cell temperatures. In fact, the ratio remained near 1.8, which is slightly higher than the 1.58 O/Ga ratio obtained from the lump of Ga_2O_3. An AES depth profile indicated that the film was uniform in composition (Figure 5.4). The surface of the Ga_2O_3 thin film remained rough and the bonding to the substrate remained weak. The surface roughness of these samples was approximately 21 nm, as shown in Figure 5.5. The substrate temperature was further lowered to 300°C which did reduce the surface roughness.

An MBE grown p-GaN substrate was also employed. The deposition was carried out at a substrate temperature of 300°C and a Ga effusion cell temperature of 840°C. The surface RMS roughness was high, 32 nm, as seen in Figure 5.6. This is partly attributed to the rough p-GaN starting surface as described in section 3.1.1. Capacitors were fabricated on this sample and the current-voltage measurement is shown in Figure 5.7. The as-deposited plot was measured prior to annealing at 500°C to improve the ohmic contact to the p-GaN. The MBE deposited Ga_2O_3 showed poor insulator properties and poor breakdown fields. Measurement of the annealed material showed that the film

degraded and the breakdown field got even smaller. Since the structural and electrical results were so poor, no further research was performed on the Ga_2O_3.

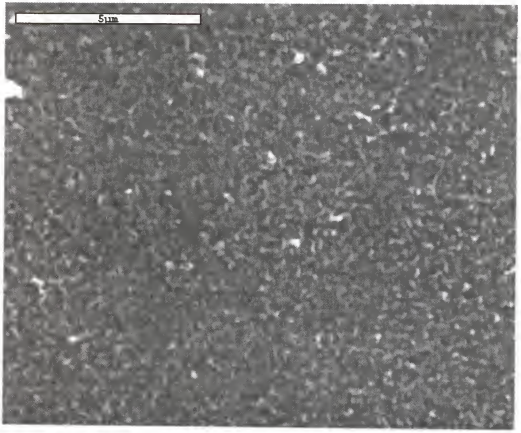


Figure 5.1 SEM image of the surface of Ga_2O_3 on Si grown at 540°C. Image was taken at 10,000x.

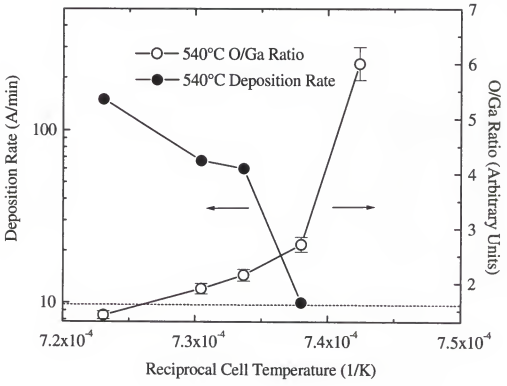


Figure 5.2 Plot of deposition rate and O/Ga ratio at a fixed substrate temperature of 540°C verses Ga cell temperature. The dashed line indicates the O/Ga ratio measured from a lump of Ga_2O_3.

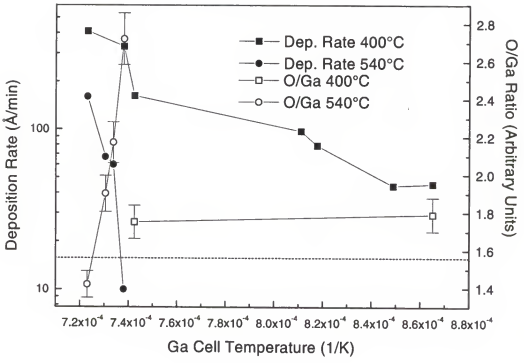


Figure 5.3 Plot of deposition rate and Ga/O ratio vs. Ga cell temperature for substrate temperatures of 400°C and 540°C. The dashed line indicates the O/Ga ratio from a Ga_2O_3 lump.

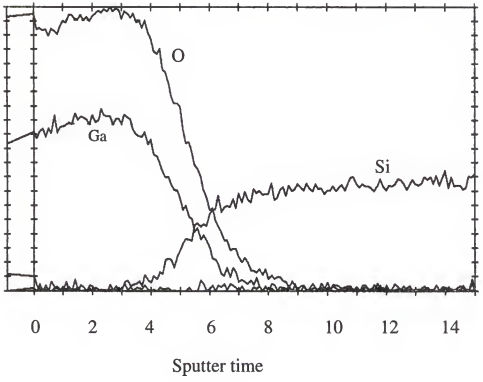


Figure 5.4 AES plot of Ga_2O_3 on Si grown at 400°C, T_{Ga}=860°C, and P_O=9x10^{-5} Torr.

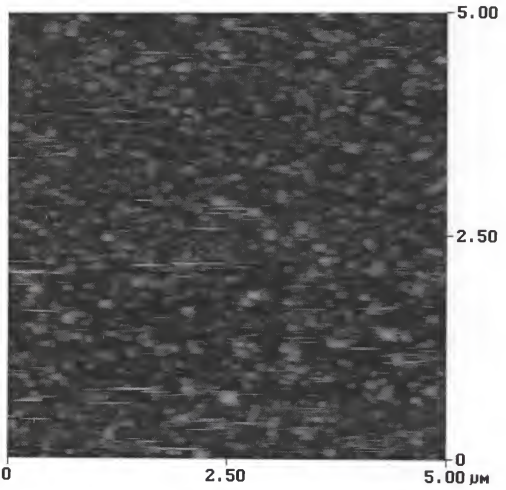


Figure 5.5 AFM image of Ga_2O_3 on Si showing large surface features. RMS roughness is approximately 21 nm.

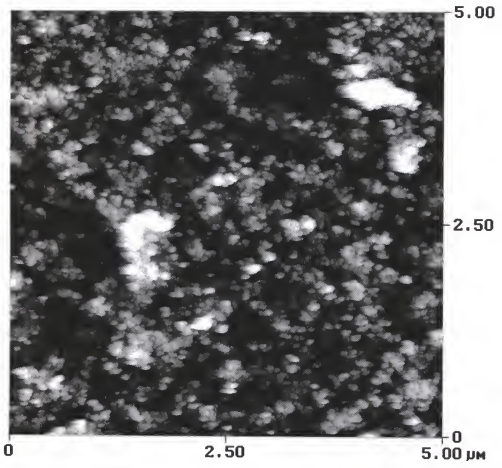


Figure 5.6 AFM image of Ga_2O_3 on MBE GaN, RMS roughness is 32 nm.

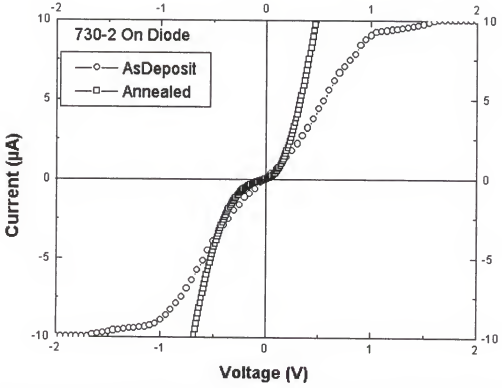


Figure 5.7 Current-voltage plot of Ga_2O_3 on GaN.

CHAPTER 6
RUSULTS AND DISCUSSION: Gadolinium Oxide

Gadolinium oxide exists in a cubic crystal structure that consists of two Fluorite-like unit cells in the three Miller directions. Oxygen atoms are located in ¾ of the tetrahedral positions in the Gd FCC array. Thus it requires two FCC cells to create a repeat unit. This is known as the Bixbyite or Mn_2O_3 structure. The (111) plane of the cubic structure will have similar symmetry to the (0001) basal plane of the hexagonal system, which is the growth face of the GaN substrates. However, there is a 20% bond mismatch between the Gd_2O_3 and the GaN.

The first Gd_2O_3 growth experiments were attempted by evaporating Gd, with the compact e-beam source, and oxygen with the ECR plasma. The low vapor pressure of the gadolinium requires a high temperature, greater than 1200°C, for deposition, therefore the e-beam source was chosen. However, it was found that the compact e-beam source became unstable when exposed to oxygen. The filament would oxidize and the power supply would call for more power. The higher power would further oxidize the filament until the power supply was at a maximum and shut down due to overload. A standard effusion cell was then used for the evaporation of gadolinium.

Growth on silicon was carried out at a gadolinium effusion cell temperature of 1200°C and an oxygen plasma setting of 200 watts forward power at $1x10^{-4}$ Torr oxygen pressure. From RHEED, the starting surface of the silicon substrate was found to be

amorphous and the Gd_2O_3 films were polycrystalline (see Figure 6.1). The polycrystalline films were smooth and uniform over a substrate temperature range of 300° to 600°C. From AFM, the surface RMS roughness was measured to be approximately 0.5 nm, as seen in Figure 6.2. These films were not weakly bonded to the substrate, as for the Ga_2O_3 films. The ratio of oxygen to gadolinium, as measured from AES surface scans, is plotted verses substrate temperature in Figure 6.3. The dashed line in the plot represents the oxygen to gadolinium ratio measured from a stable lump of 99.9% Gd_2O_3. From this plot, it can be seen that the ratio of the elements is uniform, within the error of the measurement, for the substrate temperatures used. The gadolinium source was removed from the compact e-beam source and a special conductive crucible charged with Gd_2O_3 was put in its place. The operating characteristics of the e-beam source were 60 mA at 2.5 kV. These operating parameters allowed the e-beam source to be stable over the growth of the sample. Figure 6.4 shows cross-sectional TEM of films grown on silicon substrates using the e-beam source and the elemental sources. Both samples were grown at a substrate temperature of 500°C. The deposition rate of the e-beam source was 0.5 Å/minute and the deposition rate of the elemental sources was 2.5 Å/minute. From these images, the polycrystalline morphology can be seen. Also, there appears to be a silicon oxide layer at the interface. This interface most likely formed during the indium solder mounting procedure used for the Riber MBE. Capacitors were fabricated from samples grown from the elements at substrate temperatures of 300°C and 500°C. The sample grown at 300°C showed very low forward and reverse breakdown. The results from the sample grown at 500°C are shown in Figure 6.5. From the current-voltage plot, the breakdown field was calculated to be 0.73MV/cm at 0.004A/cm^2. From

the capacitance-voltage plot, the flatband voltage shift was calculated to be 0.38V. This indicated that the gadolinium oxide grown had a low value of fixed dielectric charge. However, from the low slope of the capacitance-voltage plot, there are a large number of interface state traps present.

Once the gadolinium oxide films were shown to reproducible, experiments were conducted on GaN substrates. Since it was known from previous experiments that a clean GaN surface can be produced, section 3.1.1, the growth initiation on that surface had to be determined. Since the film being grown is a binary, there can be two different methods for producing the dielectric/semiconductor interfaces. One involved the initiation with gadolinium and the other with oxygen. Four different proceedures for growth initiation were tested on the (1x3) GaN surface produced at 700°C using these two methods.

First a low temperature 300°C exposure to the oxygen plasma was studied. RHEED images of this surface are shown in Figure 6.6. The surface changes from a sharp (1x3) to a hazy (1x2). Upon heating this sample back to 700°C without the oxygen plasma, the haziness was reduced, but the (1x2) reconstruction remained. Next, the (1x3) GaN surface was exposed to the oxygen plasma at 650°C. The surface immediately changed to the (1x2) surface seen previously, then after a 5 minute exposure to the oxygen plasma the surface became further reconstructed to a (4x4) as shown in Figure 6.7. This (4x4) surface remained after the oxygen plasma was turned off. The (1x3) surface was also exposed to a Gd atomic beam. The RHEED pattern from this surface, seen in Figure 6.8, is a (1x2). However, the spacing of the main diffracted lines has

changed, indicating that the spacing between the atoms has changed. This indicates that a different crystal structure has formed.

Growth on the low temperature oxygen plasma exposed surface initially indicated a nice Gd_2O_3 crystal structure as indicated by RHEED. The Gd_2O_3 crystal pattern formed almost immediately after the growth began. The gadolinium effusion cell temperature was 1260°C and the substrate temperature was 650°C. After 10 minutes of growth, the surface of the film had changed giving a symmetric RHEED pattern, as seen in Figure 6.9. This indicated that the Gd_2O_3 crystal quality had been reduced. The gadolinium effusion cell temperature was lowered to 1235°C to lower the growth rate and the experiment repeated. The same symmetric pattern was produced from the reduced effusion cell temperature. The surface RMS roughness of these films was 0.3 nm as seen in Figure 6.10. This is on average 1.5 times smoother than the as received MOCVD GaN. Next, growth was performed on the (1x2) GaN surface produced form the short oxygen exposure at 650°C. Here the initial Gd_2O_3 RHEED pattern remained for the duration of the growth. Extra spots were seen in the RHEED images (see Figure 6.11) indicating that the layer was partly polycrystalline. The change in the crystal structure was completely dependent on the starting substrate surface since the parameters of the growth conditions were identical. Surface RMS roughness as seen by AFM was 0.56 nm, as in Figure 6.12. Further growth experiments with reduced gadolinium effusion cell temperatures of 1210°C to 1220°C and a reduced substrate temperature of 605°C gave final RHEED patterns of the Gd_2O_3 crystal surface without the extra spots, indicating a uniform single crystal film. Samples grown on the high temperature oxygen plasma treated surface (4x4) and the gadolinium exposed surface showed sharp Gd_2O_3 crystal

RHEED patterns and smooth surfaces on the order of 0.5 nm RMS roughenss. A sample was grown using the compact e-beam source charged with Gd_2O_3 and a substrate temperature of 600°. The parameters of the e-beam were the same as those used for the silicon substrate growth. The surface RMS roughness from AFM was 0.70 nm, Figure 6.13.

From the AES depth profile in Figure 6.14, the interface between the Gd_2O_3 and the GaN was carbon free and abrupt. The ratio of oxygen to gadolinium was . The increase of oxygen at the interface could not be easily explained by AES techniques. Often in AES depth profiling, the surface atoms can be "plowed" into the next surface by the sputtering ion beam. However, the gadolinium did not show the same increase. High resolution cross-sectional TEM proved that the Gd_2O_3 grew on the GaN in a planar fashion as seen in Figure 6.15. There are dislocations visible in the image indicating that the film is highly defective. However, large areas of dislocation free material were seen in TEM. From this image, it can be seen that the Gd_2O_3/GaN interface was clean. The dark layer between the Gd_2O_3 and the GaN is a thickness effect from the ion milling process used to fabricate the TEM sample. On the left side of the image, the Gd_2O_3 lattice can be seen in contact with the GaN lattice. A lower resolution TEM image (Figure 6.16) indicated that the Gd_2O_3 planarized the GaN quite well. In fact, the Gd_2O_3 filled in the void in the GaN surface with the same registry as the entire film. Thus there was no polycrystalline morphology in the void. There were however some pockets of crystal lattice that were tilted and rotated as seen in the image. This can be attributed to the dislocations arising from the single crystal material in the void meeting single crystal material on the surface. It may be possible to reduce the dislocation density by

improving the surface quality of the GaN. X-ray diffraction of this sample showed only one peak for the Gd_2O_3 that coincided with the (111) peak from published JCPDS cards. This peak, plotted in Figure 6.17, had a shoulder to the left side and had a full width at half maximum (FWHM) of 883 arcseconds. The intensity of the x-ray system used was too low to resolve this shoulder in triple axis mode so the cause of this shoulder is unknown. X-ray diffraction of the sample that showed the extra RHEED spots (Figure 6.9) is plotted in Figure 6.18. Here a second peak was clearly seen and it corresponded to the (321) plane of Gd_2O_3. Also the FWHM of this (111) peak was over 1600 arcseconds. X-ray diffraction was also performed on the gadolinium initiated sample and the high temperature oxygen plasma initiated sample, seen in Figure 6.19. The difference in the two samples was quite large. The gadolinium initiated growth showed a FWHM of 1023 arcseconds for the (111) peak. The high temperature oxygen plasma initiated growth showed a very broad peak that was several thousand arcseconds wide. These results showed that the high temperature oxygen plasma treatment that produces a (4x4) RHEED pattern is not the ideal surface to initiate growth.

A thermal stability experiment was performed on the sample that gave the 883 arcsecond FWHM. This sample was chosen since it gave the lowest FWHM and would be more sensitive to crystal degradation. The sample was annealed at 1000°C for 30 seconds under flowing nitrogen. The surface RMS roughness of the annealed sample was 0.60 nm seen in Figure 6.20. This is less than a 10% increase in RMS roughness from the as grown surface RMS roughness of 0.56 nm. An AES depth profile (Figure 6.21) showed that the interface between the Gd_2O_3 and the GaN remained abrupt and there was no diffusion of either oxygen or gadolinium into the GaN surface. This showed that the

interface was stable up to 1000°C. There was also a smoothing of the oxygen signal in the depth profile, however, the oxygen increase at the interface was still present. X-ray diffraction from this annealed sample gave a FWHM of 789 arcseconds as seen in Figure 6.22. This was almost 100 arcseconds less than the as grown sample. This indicated that the 1000°C anneal improved the crystal quality without degrading the interface or surface.

Electrical measurements were carried out on these samples. The best breakdown field measured from Gd_2O_3 grown on n-GaN was 0.55MV/cm, seen in Figure 6.23. A depletion mode MOSFET was fabricated using the Gd_2O_3 as the gate dielectric. The dielectric thickness was 70.0 nm and the gate dimensions were 1 μm x 200 μm. The MOSFET fabricated was able to modulate the GaN beneath the gate to turn "off" the transistor. A plot of the drain current verses the source-drain voltage for different gate voltages indicated that the transistor was turned "off" at a gate voltage of –4.0v, as seen in Figure 6.24. However, when the gate bias is increased above 0 V to increase the carrier concentration in the channel, leakage from the channel through the gate dielectric is observed as indicated in Figure 6.25. This leakage was reduced with the addition of silicon oxide deposited by electron beam evaporation on top of the gadolinium oxide. This showed that the bulk of the oxide was highly defective, but the dielectric/semiconductor interface quality was good.

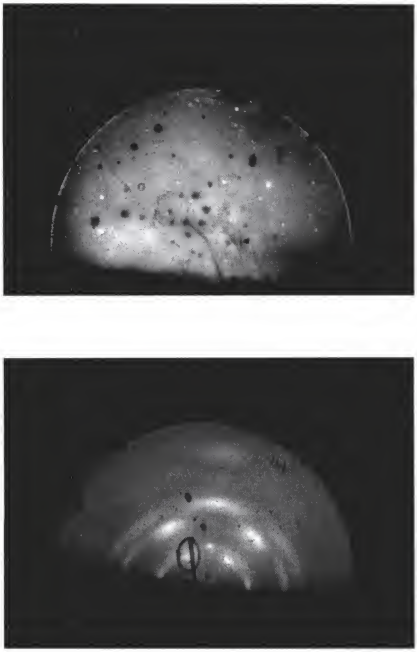


Figure 6.1 RHEED image of (a) Si with native oxide and (b) Gd_2O_3 grown at 500°C from elemental sources.

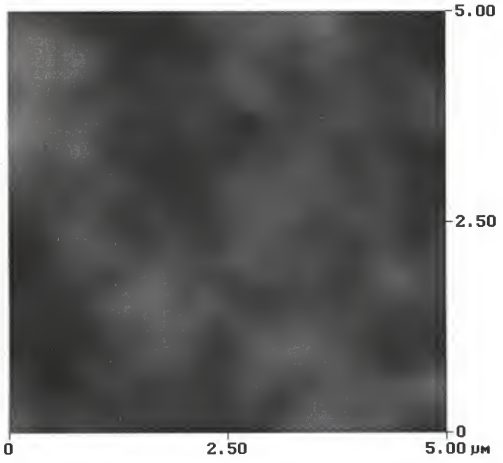


Figure 6.2 AFM image of Gd2O3 on Si grown at 500°C. RMS roughness is approximately 0.5 nm.

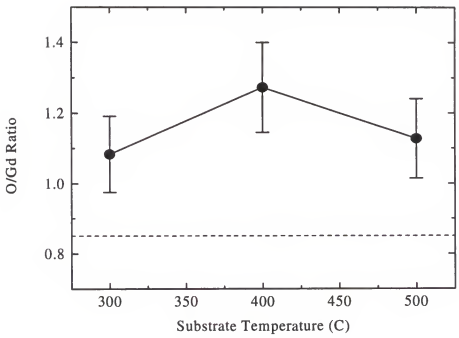
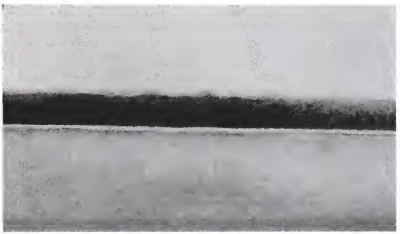
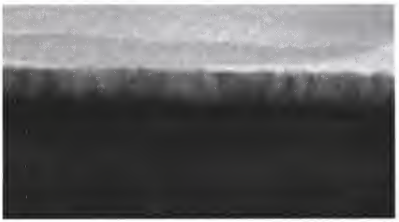


Figure 6.3 Plot of oxygen to gadolinium ratio verses substrate temperature for films grown on Si. Dashed line represents the O:Gd ratio measured from a Gd_2O_3 lump.

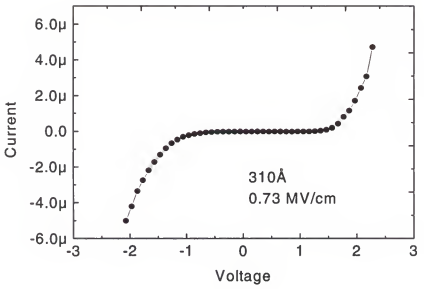


(a)

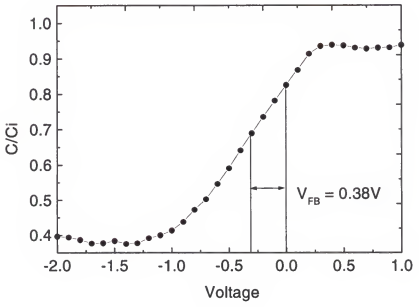


(b)

Figure 6.4 TEM image of Gd_2O_3 on Si grown at 500°C, from (a) e-beam evaporation of Gd_2O_3 and (b) elemental sources. Film thickness are 10nm and 15nm, respectively.



(a)



(b)

Figure 6.5 Plots of (a) current-voltage and (b) capacitance-voltage measurements of Gd_2O_3 on Si. The sample was grown at 500°C.

(a)

(b)

Figure 6.6 RHEED images of (a) a (1x3) GaN surface at 700°C and (b) the same surface at 300°C under O plasma, showing a (1x2). The left is the <11-20> and the right is the <1-100>.

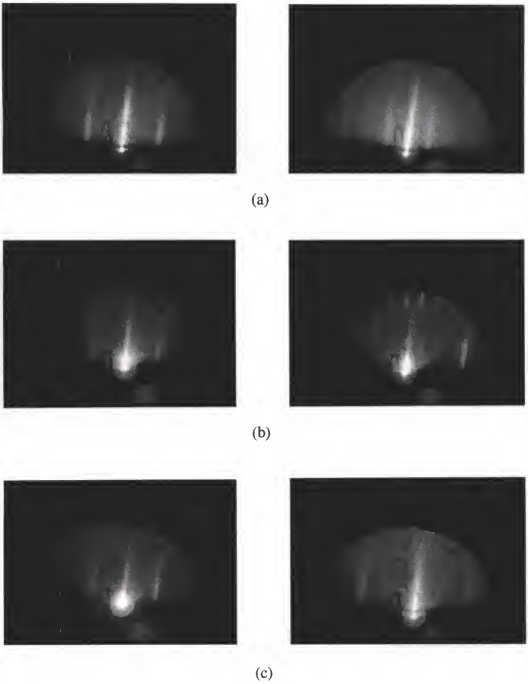


Figure 6.7 RHEED images of (a) a (1x3) GaN surface at 700°C , (b) the same surface after receiving an O plasma exposure for 5 minutes at 700°C, showing a faint (4x4), and (c) a (1x1) Gd_2O_3 grown at 610°C on the (4x4) oxygen treated surface. The left is the <11-20> and the right is the <1-100>.

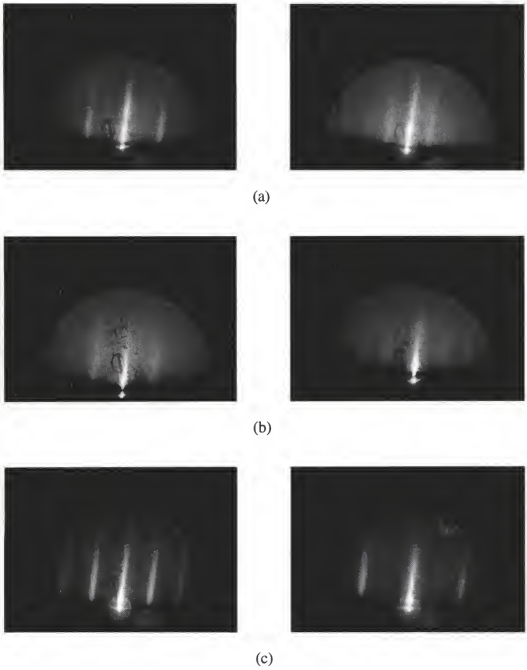


Figure 6.8 RHEED image of (a) a (1x3) GaN surface at 700°C, (b) Gd exposure for 1 minute at 650°C, and (c) a (1x1) Gd_2O_3 surface grown at 610°C. The left is the <11-20> and the right is the <1-100>.

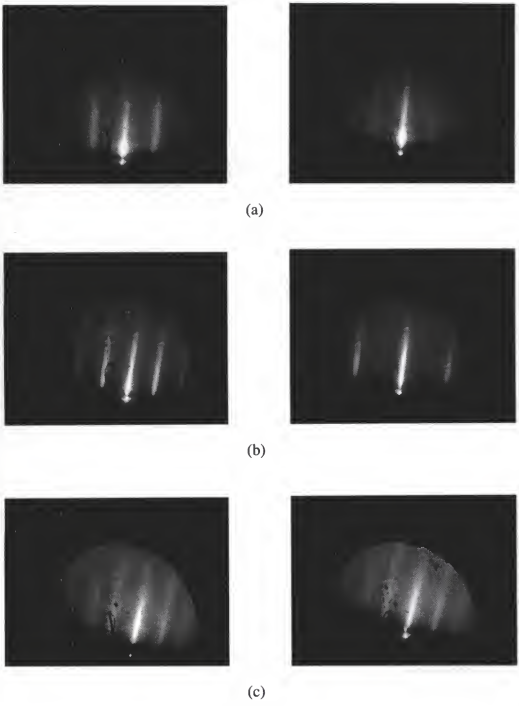


Figure 6.9 RHEED images of (a) a (1x2) oxygen treated GaN surface, (b) a (1x1) Gd_2O_3 surface after 10 minutes of growth, and (c) a symmetric pattern of Gd_2O_3 after 90 minutes of growth. The left is the <11-20> and the right is the <1-100>.

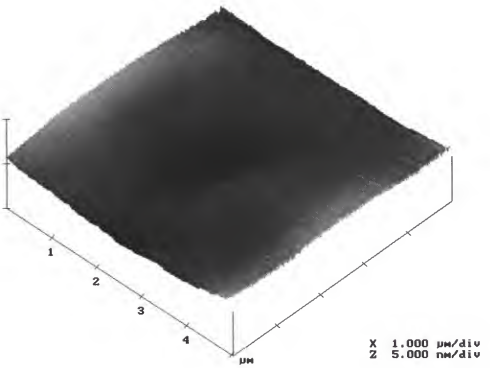


Figure 6.10 AFM image of Gd_2O_3 on GaN grown at 650°C. RMS roughness is approximately 0.3nm.

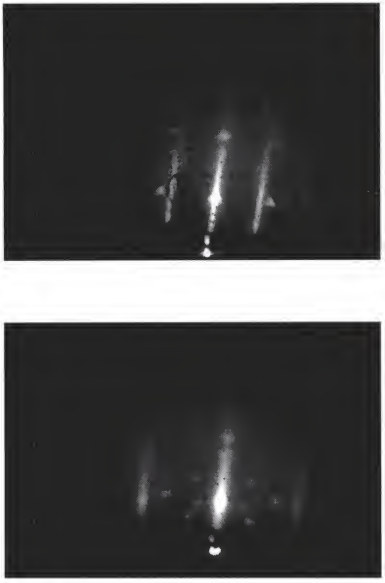


Figure 6.11 RHEED image of Gd_2O_3 (1x1) indicating extra spots due to defects. The top image is taken from the <11-20> crystal direction and the bottom image from the <1-100> direction.

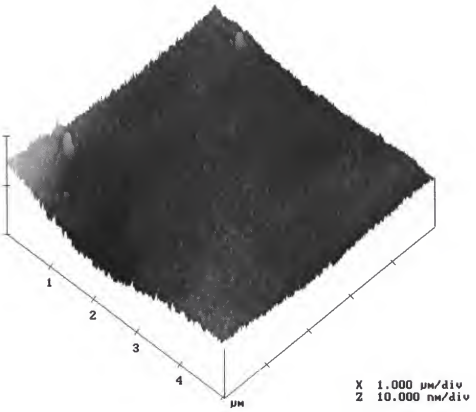


Figure 6.12 AFM image of Gd_2O_3 grown at 650°C on GaN. Surface RMS roughness is 0.56nm.

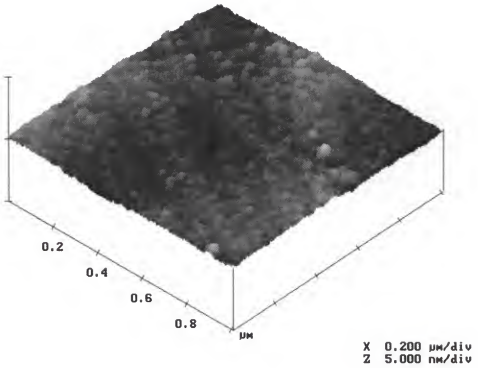


Figure 6.13 AFM image of Gd_2O_3 grown on GaN at 600°C from e-beam source. Surface RMS roughness is 0.70nm.

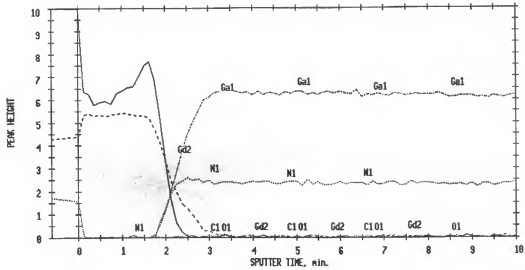


Figure 6.14 AES plot of Gd_2O_3 grown on GaN at 650°C from elemental sources.

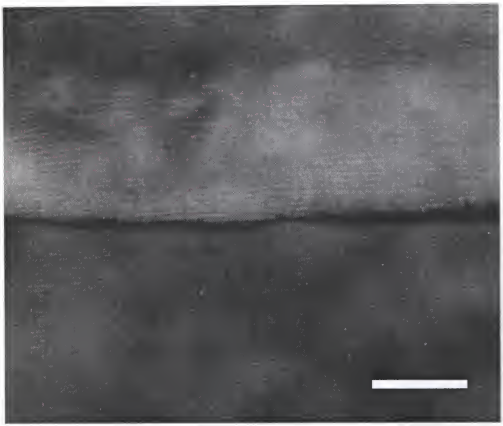


Figure 6.15 TEM image of Gd_2O_3 on GaN. The GaN is on bottom and Gd_2O_3 is on top. Notice the difference in lattice spacing. The bar length is 5.0nm.

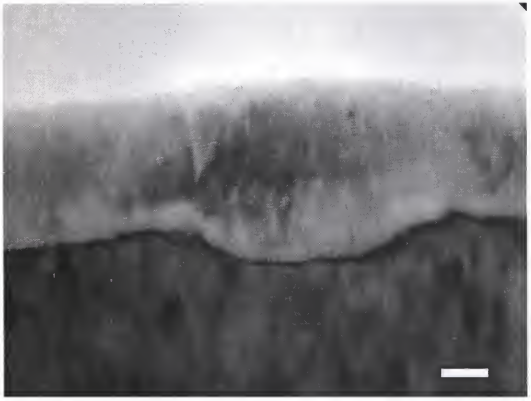


Figure 6.16 TEM image of Gd_2O_3 on GaN grown at 650°C from elemental sources. Bar length is 5.0 nm.

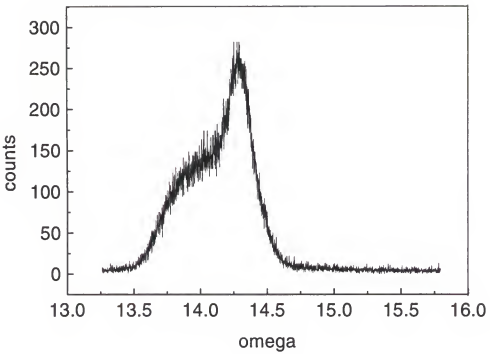


Figure 6.17 X-ray diffraction plot of Gd_2O_3 grown on GaN at 650°C. The FWHM of the peak is 883 arcseconds.

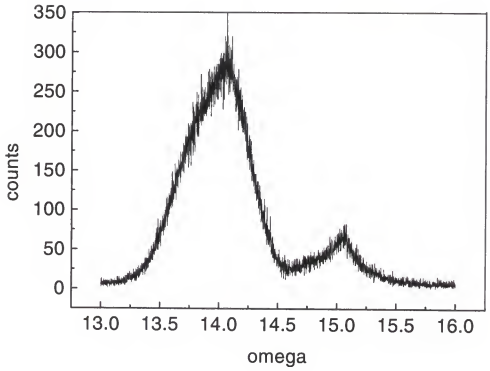


Figure 6.18 X-ray diffraction of Gd_2O_3 on GaN with extra diffraction spots from RHEED. The FWHM of the main peak is 1623 arcseconds.

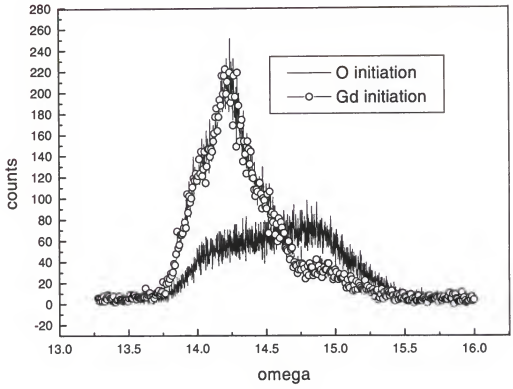


Figure 6.19 X-ray diffraction plot of samples grown on a Gd exposed GaN surface and a high temperature O plasma exposed GaN surface. The FWHM of the Gd initiated sample is 1058 arcseconds.

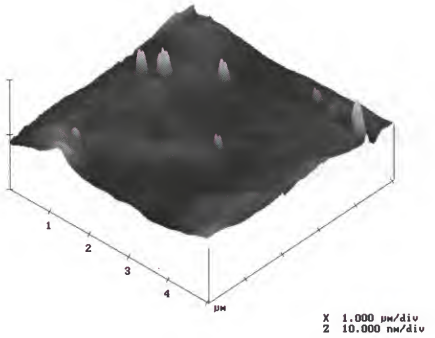


Figure 6.20 AFM image of Gd_2O_3 on GaN grown at 650°C after receiving a 1000°C RTA anneal under nitrogen. Surface RMS roughness is 0.60nm.

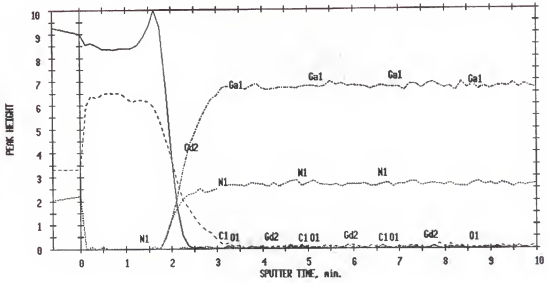


Figure 6.21 AES plot of Gd_2O_3 grown on GaN at 650°C and receiving a RTA anneal at 1000°C under nitrogen.

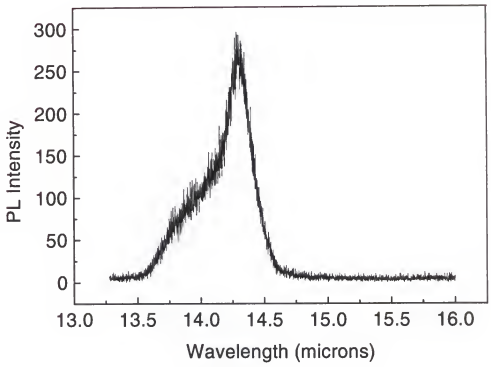


Figure 6.22 X-ray diffraction plot of Gd_2O_3 grown at 650°C (same as in figure 6.17) after a 30 second 1000°C anneal in nitrogen. The FWHM of the peak is 789 arcseconds.

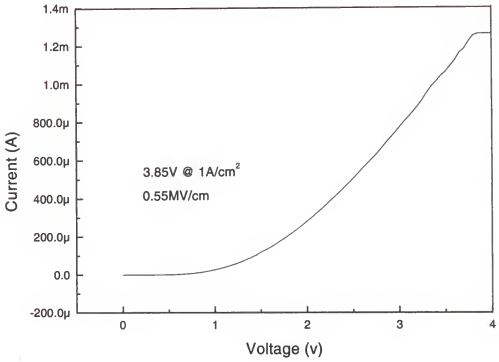


Figure 6.23 Current-voltage plot of Gd_2O_3 on GaN grown at 650°C. Sample was 70 nm thick.

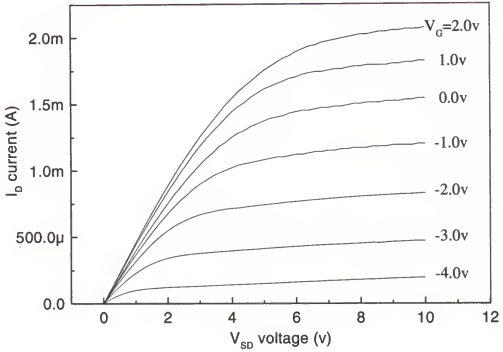


Figure 6.24 Plot of drain current (I_D) verses source-drain voltage (V_{SD}) for different gate voltages (V_G). The transistor turned "off" at a gate voltage of –4.0v.

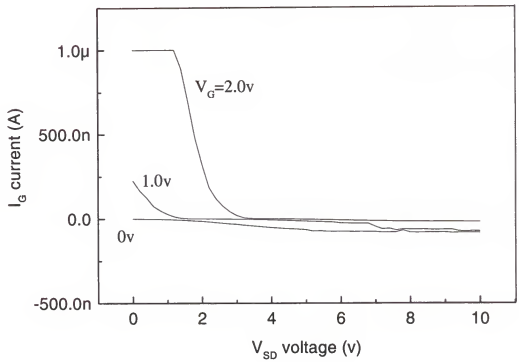


Figure 6.25 Plot of gate current (I_G) verses source-drain voltage (V_{SD}) for different gate voltages (V_G). Gate current leakage occurs when positive bias is applied.

CHAPTER 7
RESULTS AND DISCUSSION: Magnesium Oxide

Magnesium oxide was chosen as a possible dielectric material for GaN for its high melting point (2850°C) and large band gap (7.3 eV). The structure of MgO is the NaCl crystal structure, Figure 7.1. This is a cubic structure with a lattice constant of 4.20Å. The symmetry alignment for MgO:GaN is the MgO (111) and the GaN (0001). The cation spacing for the MgO (111) plane is 2.97Å and for the GaN (0001) plane is 3.19Å this gives a mismatch of 6.9%, as shown in Figure 7.2. This is much less than the mismatch between the Gd_2O_3 (111) and the GaN (0001). Given the success of the highly mismatched Gd_2O_3 growth on GaN, MgO was also pursued.

Magnesium oxide sample growth was described in section 3.1.5. Initial samples were grown on Si substrates. It was determined by AES that an effusion cell temperature of 400°C gave significant growth and a temperature of 350°C gave no growth of MgO. In both cases, the oxygen plasma conditions were identical. This established an effusion cell temperature regime for growth on GaN.

The MgO growth on GaN was performed at a substrate temperature of 650°C. The RHEED images in Figure 7.3 show the results of the first attempt to grow MgO on GaN. The effusion cell temperature was 400°C. The growth rate for this condition was 28.9 Å/minute. From the RHEED images, the pattern taken at 1 minute, Figure 7.3(b), indicate that the growth initiated with a single crystal orientation. However, as seen in

Figure 7.3(c), the final crystal structure was polycrystalline. The surface RMS roughness determined by AFM was 9.7 nm, as shown in Figure 7.4. An AES surface scan of this sample showed no contamination within the detection limits of the AES system and an oxygen to magnesium ratio of approximately 1.5 (see Figure 7.5).

Electrical measurements were also made on this sample. The sample was masked with photoresist and etched using 85% phosphoric acid at room temperature to expose the n-GaN for ohmic contact formation. The etch procedure took only a few minutes to remove the 2600Å of MgO. Current-voltage measurements showed that the sample had a large forward breakdown of about 18 V at 1 A/cm^2 current density (see Figure 7.6). The breakdown field was calculated to be 0.69 MV/cm. This value is lower than that obtained from the Gd_2O_3 and is likely due to the polycrystalline nature of the dielectric. Once the breakdown voltage was exceeded, the measurement was repeated. This time, the breakdown voltage was found to be 1.3 V at 1A/cm^2. This gave a breakdown field of 0.05MV/cm. The grain boundaries of the polycrystalline dielectric are the likely culprit of both the low breakdown field and the shorting failure of the magnesium oxide. A reduction in the grain boundary population by enlarging the grains or eliminating the grains by producing a single crystal film should lead to improvements in the dielectric.

A second sample was grown using a reduced effusion cell temperature of 360°C to try to reduce the growth rate. The growth rate using this effusion cell temperature was 5.6 Å/minute. The RHEED image of this film, shown in Figure 7.7, shows that the surface is less polycrystalline than the previous sample grown at the higher effusion cell temperature. This may be due to the reduced growth rate or maybe simply be due to the reduced film thickness. Cross-sectional TEM or powder x-ray diffraction is needed to

clarify this. An AFM image of this sample showed the surface roughness to be 4.1 nm, (see Figure 7.8). Again, this can be attributed to the thinner film and not necessarily the slower growth rate.

Further research in this area is needed to determine the parameters of high quality crystal growth. A reduction in substrate temperature will most likely increase the growth rate and allow for more magnesium to "stick" to the surface. The growth conditions used thus far allowed for the magnesium atoms impinging on the surface to have a short residence time on the surface. This is due to the vapor pressure of magnesium being higher at the substrate surface (650°C) than in the effusion cell (360° to 400°C). The magnesium atoms have to be incorporated into the film by the impinging oxygen atoms. This growth mode tends to inhibit the mobility of the magnesium atom on the surface, prohibiting it from locating an energetically favorable adatom site. If a lower substrate temperature is used, the residence time and thus the surface migration of the magnesium atoms will be increased. This should allow for a higher crystal quality and thus a higher quality dielectric material.

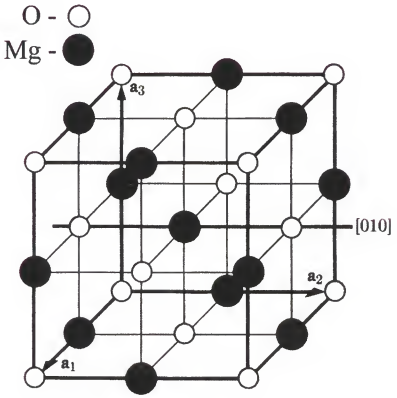


Figure 7.1 Illustration of the MgO structure (from Cullity 1978)

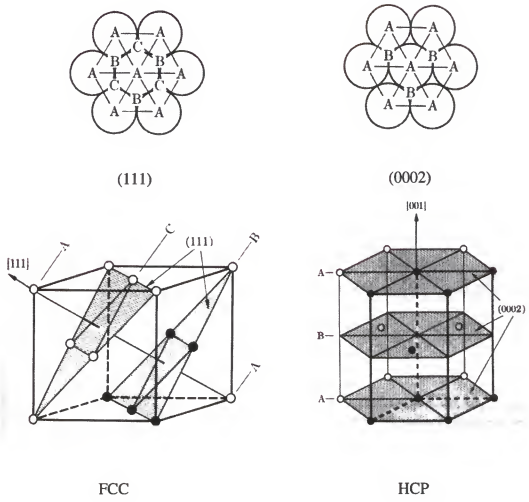
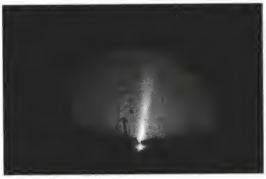
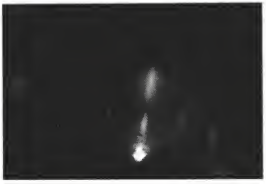


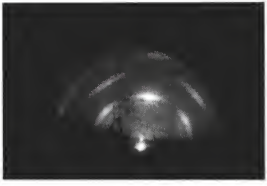
Figure 7.2 Illustration showing the symmetry between the (111) NaCl plane and the (0002) wurtzite plane. The spacing between atoms marked A is 2.97Å for NaCl MgO and 3.19Å for wurtzite GaN.



(a)



(b)



(c)

Figure 7.3 RHEED images indicating (a) the starting GaN surface, (b) MgO after 1 minute of growth, and (c) MgO after 90 minutes of growth. Growth temperature is 650°C.

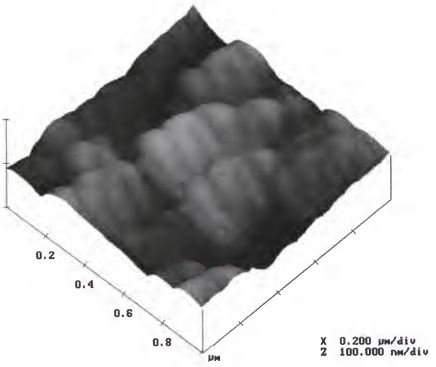


Figure 7.4 AFM image of MgO on GaN grown at 650°C. RMS roughness is 9.7nm.

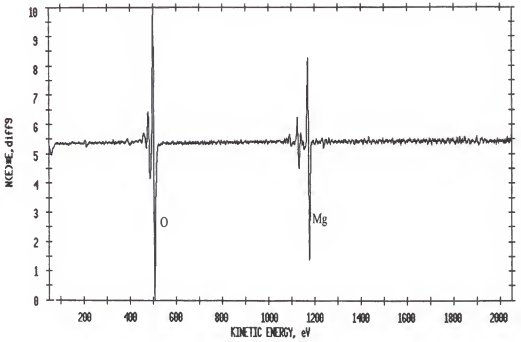


Figure 7.5 AES surface scan of MgO on GaN grown at 650°C. The peak to peak ratio indicates a O:Mg ratio of 1.5.

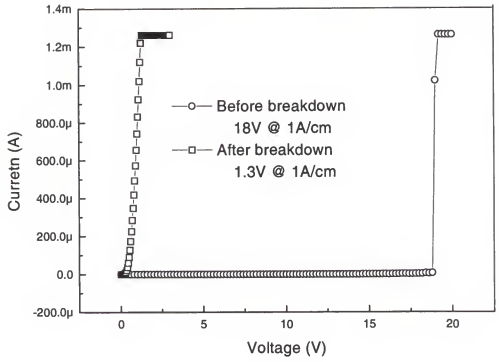
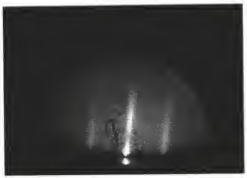
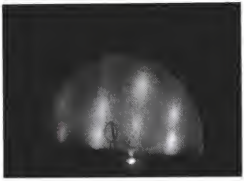


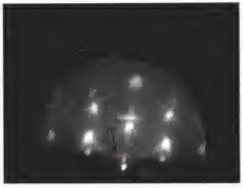
Figure 7.6 Plot of current-voltage of MgO on n-GaN, shows before and after breakdown measurements.



(a)



(b)



(c)

Figure 7.7 RHEED images of (a) (11-20) GaN surface, (b) MgO after 10 minutes of growth, and (c) MgO after 90 minutes of growth. Mg effusion cell temperature was 360°C.

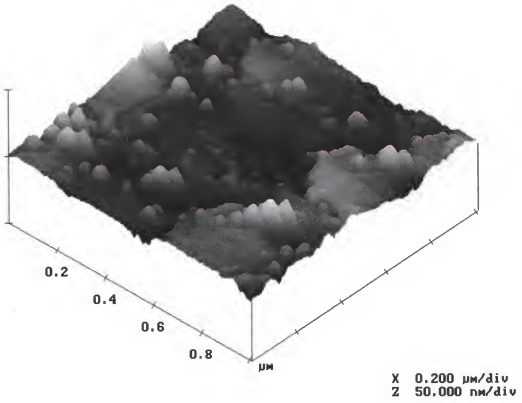


Figure 7.8 AFM image of MgO grown at 650°C on GaN using an effusion cell temperature of 360°C. The surface RMS roughness is 4.1 nm.

CHAPTER 8
SUMMARY AND CONCLUSIONS

In order to fabricate a high quality dielectric material, control of the growth and preparation of the interface between the dielectric and semiconductor must be understood. Four different growth initiations and four dielectric materials were studied.

Aluminum nitride showed very good elemental ratio and microstructural control when grown on silicon. The surface was extremely smooth and annealing decreased the flat band voltage shift on silicon. Results of aluminum nitride grown on SiC at 325°C showed that the dielectric material preformed well. The breakdown field was the highest achieved in this study at 6.8 MV/cm and elevated temperature capacitor testing showed that the dielectric had no thermal history up to 300°C. Future work on aluminum nitride should involve substrate temperatures below 325°C to create a completely amorphous AlN film. To do this, an aluminum effusion cell as an aluminum source would be required. The metal-organic aluminum source used in this dissertation required a minimum substrate temperature of about 325°C to decompose the molecule. This temperature gives a mixed amorphous/crystalline structure.

The gallium oxide dielectric material produced in this study showed poor elemental ratio control, weak physical structure and substrate bonding and poor electric insulating properties. A large range of silicon substrate temperatures and gallium effusion cell temperatures were attempted with no promising results. When grown on

GaN, the results were still poor. There are no future experiments planned for gallium oxide.

By contrast, gadolinium oxide showed very promising results. The stoichiometry of the oxide was stable over a growth temperature range of 300°C to 650°C. The single crystal structure and the electrical properties of the gadolinium oxide were stable as well. This study was the first reported growth of Gd_2O_3 by elemental sources by MBE. The surface RMS roughness of the gadolinium oxide showed that it grew smoother than the GaN. From the MOSFET device results, it was shown that the Gd_2O_3/GaN interface was of good quality, however, the bulk of the oxide showed leakage. Dislocations in the bulk of the oxide are believed responsible for the current leakage. A lower surface RMS of the gallium nitride should help to reduce the number of defects in the bulk of the gadolinium oxide. Future work in this field should be concentrated in planarizing the GaN surface through ex-situ preparation. Also future work involving the use of SiC substrates should be planned. From the AlN on SiC results, lower surface RMS roughness of the semiconductor lead to higher device quality. The SiC has a surface roughness of 0.1 nm compared to the GaN surface RMS roughness of 1.0 nm to 3.0 nm. Also future experiments incorporating another type of cation or perhaps nitrogen to form a mixed oxide or an oxynitride from elemental sources may produce a higher quality dielectric.

The magnesium oxide experiments showed that the oxide could be grown by a conventional MBE technique. The dielectric showed a breakdown field of only 0.65 MV/cm, which is comparable to the gadolinium oxide results of 0.55 MV/cm. It is believed that the same problems that plagued the gadolinium oxide samples are

responsible for the low breakdown fields of the magnesium oxide: the rough MgO/GaN interface and high dislocation density. Future work on the magnesium oxide should be focused on employing SiC substrates, due to their lower surface RMS roughness and a better lattice match.

APPENDIX 1
IDEAL AND REAL DIODES

A1.1 Ideal MIS diode measurments

Figure A1.1 shows the energy band diagram for an ideal MIS, which is defined as the case where the energy difference between the metal work function, Φ_m, and the semiconductor work function, Φ_s, is zero at zero applied bias. The metal-semiconductor work function difference, Φ_{ms}, is expressed as

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} - \Psi_B \right) = 0 \qquad \text{for n - type}$$

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} + \Psi_B \right) = 0 \qquad \text{for p - type}$$

where χ is the semiconductor affinity, χ_i, the insulator electron affinity, E_g the bandgap, Φ_B the potential barrier between the metal and the insulator, q the charge of electron, and Ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i.

A1.2 Equations for Capacitance–Voltage Plot

When an MIS capacitor is in accumulation, the total capacitance measured is the insulator capacitance, total capacitance C_i and given by equation

$$C_i \left[\frac{\mathrm{F}}{\mathrm{cm}}\right] = \frac{\varepsilon_i}{d}$$

where ε_i is the insulating layer dielectric constant and d is the thickness of insulator layer. In depletion the capacitance drops with increasing gate voltage, V_G due to the development of a depletion region in the semiconductor surface. In a depletion layer the overall capacitance, consisting of a series connection of the insulator capacitance, C_i and the capacitance across the depletion layer, C_s, is given as

$$\frac{1}{C} = \frac{1}{C_s} + \frac{1}{C_i}$$

The flatband voltage, V_{FB} is defined as the voltage where the energy bands are flat, and this is determined by the metal–semiconductor work function difference, Φ_{ms}, and the total charge in the insulator layer and in the interface states, Q_i.

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$$

To determine the experimental flatband voltage, the flat band capacitance for the semiconductor, C_{FBS}, relative to the capacitance, C_i, must first be calculated from the insulator thickness, d, epilayer doping concentration N, the dielectric constant for the semiconductor, ε_s, and the Debye length, L_D.

Doping concentration can be extracted from a plot of $1/C^2$ versus V. Since the curve is a straight line in the plot, this indicated the doping was constant.

$$N = \frac{2}{q\varepsilon_s A^2}\left[\frac{1}{\partial\left(1/C^2\right)/\partial V}\right]$$

$$L_D = \sqrt{\frac{k_B \cdot T \cdot \varepsilon_s}{q^2 N}}$$

$$C_{FBS} = \frac{\varepsilon_s \cdot A}{L_D}$$

where k_B is Boltzmann constant and T is the temperature in Kelvin. The overall flatband capacitance is given by

$$C_{FB} = \frac{C_{FBS} \times C_i}{C_{FBS} + C_i} = \frac{1}{1 + \frac{\varepsilon_i \cdot L_D}{\varepsilon_s \cdot d}}$$

For calculating the voltage shift, the C/C_i versus voltage plot was obtained. Then the ratio of C_{FB}/C_i was used to calculate the flatband voltage shift, V_{shift} or ΔV. In an ideal MIS diode, the flatband capacitance occurs at $V_{shift} = 0$, where $\psi_s = 0$. Figure A1.2 summarizes the MIS capacitance–voltage curves for the cases of low frequency, high frequency, and deep depletion. Once V_{shift} is known, the interface state density, N_{DIT} will be calculated by

$$N_{DIT} = \left(\frac{V_{shift} - \Phi_{ms}}{q}\right) \cdot C_i$$

A1.3 High-frequency measurements

Majority carriers respond to changes in the electric field with a time known as the dielectric relaxation time. This is the time within which majority carriers are

redistributed in response to an electric disturbance. It is given by the ratio of the dielectric constant to the conductivity, ε/σ. For semiconductors, such as Si and GaAs, having a resistivity of 1 Ω–cm, this time is of the order of 10^{-12} second. Therefore, at the frequency of the ac signal voltage, corresponding to a period of 1 μs, majority carriers will have no trouble responding to the variation in ac signal.

Minority carriers in the MIS capacitor form an inversion layer at the surface of the insulator and originate by generation in the bulk, take a fraction of a second to form the inversion layer. Therefore, at the frequency of 1 MHz and an AC signal period of 1 μs, it is not possible for the inversion layer to acquire a difference in total charge due to the minority carrier in response to the AC signal voltage.

Depending on the gate bias the MIS capacitor has three distinct operation modes: a) accumulation, b) depletion, and c) inversion. Figure A1.3 illustrates the energy band diagrams when $V_G \neq 0$ for the three conditions. In accumulation, majority carriers are accumulated at the interface between insulator and semiconductor, and this concentration is larger than the doping concentration in the bulk immediately below. The intrinsic Fermi level has moved further away from E_F and an accumulation layer is formed. The capacitance measured in this case is just the capacitance of the insulator film. In depletion or deep depletion, majority carriers are depleted from the semiconductor immediately below the insulator. As the bias is increased, the energy bands bend far enough for E_i to be equal to E_F at the surface. The depleted semiconductor will act as a capacitance in series with the insulator capacitance, thus lowering the measured capacitance value. During inversion, minority carriers will be collected at the interface between the semiconductor and insulator due to the excessive band bending. With

further increase in the bias voltage, E_i dips below E_F. Further depletion of the semiconductor is inhibited beyond a certain limit, due to screening of the electric field by the inversion layer charge and capacitance measurements will show a minimum capacitance. Figure A1.4 illustrates the high frequency C-V plot for a p-type substrate.

A1.4 Low frequency measurements and deep depletion

During a low frequency measurement, the accumulation and depletion regions of the capacitance-voltage curve are identical. The inversion region of the low frequency capacitance-voltage plot, Figure A1.2, however, rises up to the C_i value. This occurs because the minority carrier concentration can change rapidly enough to follow the low frequency of the measurement.

During deep depletion, the minority carriers cannot be accumulated at the oxide/semiconductor interface or are generated too slowly. There are two possible reasons for deep depletion. One reason is the insulator leaks the minority carriers to the metal/insulator interface and they recombine with the charge accumulated there. The second reason is the generation of minority carriers in the semiconductor is very slow, as in a low temperature capacitance measurement.

A1.5 Real MIS diode measurements

Real capacitance-voltage measurements differ from ideal measurements by a parallel shift or distortion of the plot. A parallel shift along the d.c. applied voltage axis indicates the presence of trapped space charges distributed in the insulator layer and are

time invariant during the measurement. These are generally termed fixed dielectric charges. However, these traps are not fixed and can migrate through the dielectric in an applied field. A negative gate voltage shift results from a positive oxide charge and a positive gate voltage shift results from a negative oxide charge. This will occur on both n-type and p-type substrates and is independent of the semiconductor.

A distortion along the applied voltage axis is an indication of charged traps located at the oxide/semiconductor interface or in the surface space-charge layer. These are termed charged interface traps. The distortion is caused by the voltage dependences of the density of the trapped interface charge when the applied voltage is varied. Figure A1.5 illustrates both the parallel shift and the distortion of the capacitance-voltage plot compared to an ideal diode.

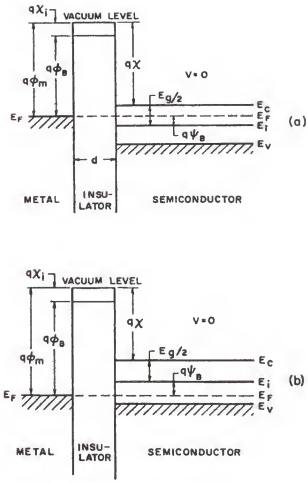


Figure A1.1 Energy band diagrams for ideal MIS diodes at V_G=0 for (a) n-type and (b) p-type (after Sze).

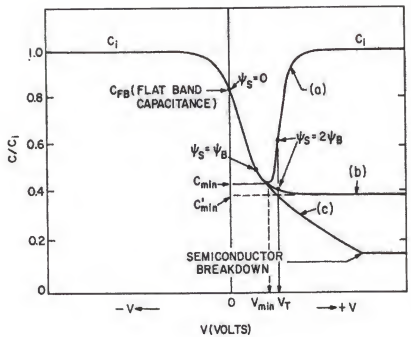


Figure A1.2 MIS capacitance-voltage curves for (a) low frequency, (b) high frequency, and (c) deep depletion (after Sze) Graph depicts a p-type semiconductor.

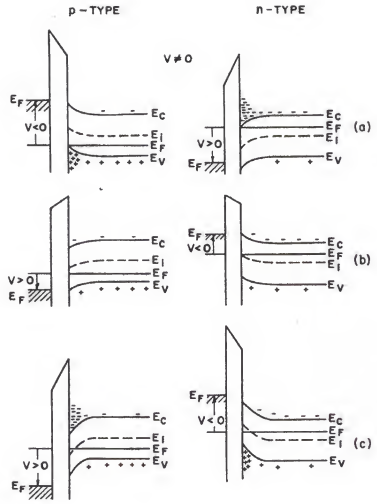


Figure A1.3 Energy band diagrams for ideal MIS diodes when V_G not equal 0, for (a) accumulation, (b) depletion, and (c) inversion (after Sze).

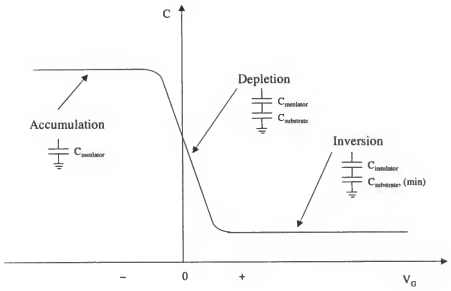


Figure A1.4 High frequency capacitance-voltage measurement for an ideal diode.

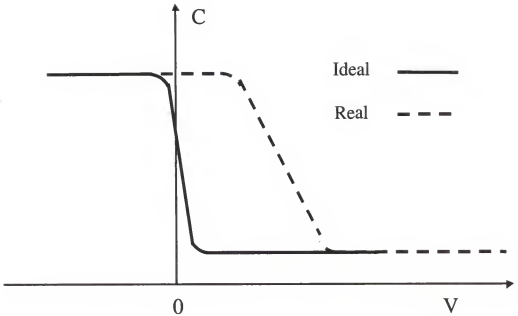


Figure A1.5 Illustration of an ideal and a real capacitance-voltage plot.

APPENDIX 2
RHEED ANALYSIS

Reflection high energy electron diffraction (RHEED) patterns are obtained from electrons diffracting from a surface. The typical geometry of a RHEED system is illustrated in Figure A2.1. Electron beam energy ranges from 5 kV to 25 kV. These energies are high enough to cause damage to the surface if the electron beam was normal to the surface. With the angle between the beam and sample being only 1° to 2°, the fraction of the energy normal to the surface is small. This is determined by equation A2.1 where E_{normal} is the energy normal to the sample surface, E_{beam} is the incident electron beam energy and θ is the angle between the sample surface and the incident electron beam.

$$E_{normal} = E_{beam}(\sin \theta) \qquad \text{A2.1}$$

An incident beam energy of 10 kV allows for only 0.350 kV of energy entering the surface. This gives a penetration depth of the radiation is only a few atomic layers and makes this technique very surface sensitive.

Diffraction of cubic and hexagonal (001) type planes are typically taken from two different angles, 90° apart, to create a 2-dimensional map of the surface. Figure A2.2 shows an illustrated image of the surface, indicating the directions used for the RHEED

patterns. If one looks down the arrows, the rows of atoms and the difference in the spacing between these rows of atoms is seen. Examples for RHEED patterns are seen in Figure A2.3. These two patterns are taken 90° apart from each other. Initially, the patterns appear backwards, but the diffraction images are in reciprocal lattice spacing, so the closer the atoms are in real space, the farther apart they appear in reciprocal space. Since there are no atoms missing, the surface diffraction is the same as the bulk diffraction therefore this surface is called a (1x1). Here the first crystal direction is the <11-20> and the second is the <1-100>.

When atoms are missing from the surface, the RHEED pattern changes. This is illustrated in Figure A2.4. Here, two rows of atoms are missing in the <1-100> direction and will be indicated by extra lines appearing in the diffraction pattern. This shows as the (1x3) diffraction pattern seen in Figure A2.5. The bright diffraction lines are due to the complete underlying atom layer and the weaker lines are due to the diffraction of the surface atoms. If more rows of atoms are missing, more lines appear in the diffraction pattern. These extra lines are between the main diffracted line and the bulk diffracted line at a spacing that is equal to the number of extra lines. Again, realizing that the diffraction pattern is of a reciprocal lattice, the farther apart the next row of atoms, the closer it will be to the main diffracted line.

In these examples above, the surface of the sample is assumed to be smooth. This however is not always the case. As the surface roughness increases, the long streaky lines of the RHEED pattern become elongated ovals, and eventually become a series of spots in a row. This can indicate if the growth mode is either step flow (smooth) or 3-dimensional islanding (rough). This information is used to tailor the growth conditions.

Also the intensity of the reflected electron beam can be measured to indicate a growth rate. When the reflected spot is at maximum intensity, the surface is the smoothest, indicating a complete coverage of atoms. The intensity will decrease to a minimum value when the surface is ½ covered with atoms. Then the intensity will increase as the surface coverage returns to 100%. This repeats again as the next layer forms. From these oscillations in intensity and a post grown thickness measurement, a precise growth rate can be calculated for each oscillation, allowing for complex multi-layer structures to be grown.

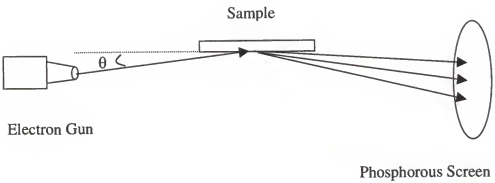


Figure A2.1 Illustration of a RHEED apparatus. Shown are the electron beam paths, both incident and diffracted, indicated by the arrows. The electron gun, sample , and phosphorous screen are located inside the ultra-high vacuum chamber. The incident electron beam angle, θ, is approximately 1° to 2°.

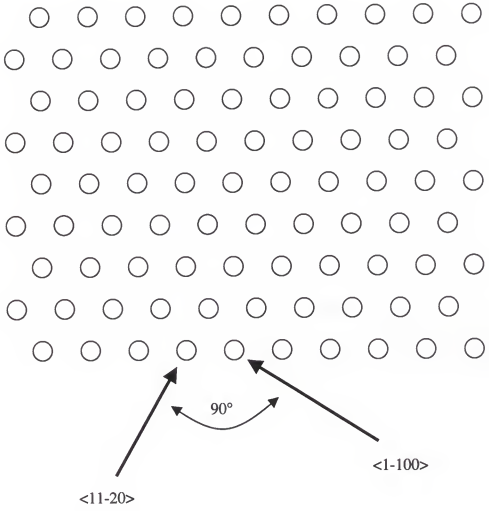
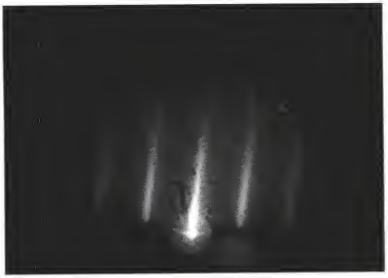
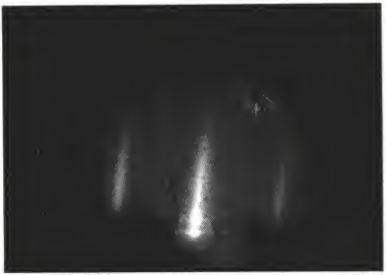


Figure A2.2 Illustration of the (0001) plane of a hexagonal crystal. Arrows indicate the two crystal directions used to obtain the RHEED diffraction patterns. The "circle" symbols indicate atom positions on the surface that are also in the bulk.



(a)



(b)

Figure A2.3 RHEED examples of (a) <11-20> direction and (b) <1-100> direction. This is termed a (1x1) image due to the lack of extra diffraction lines.

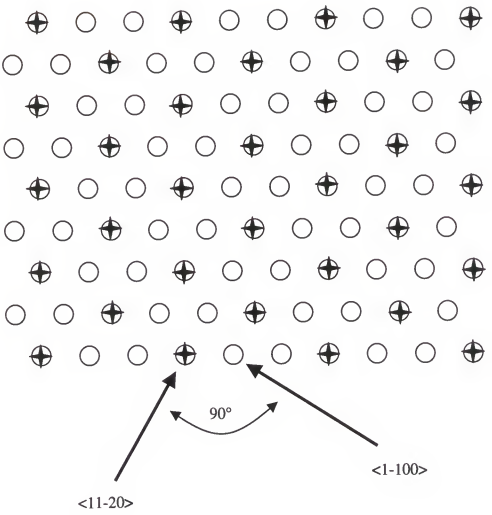
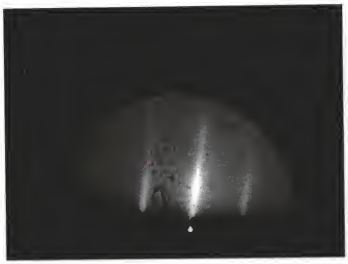
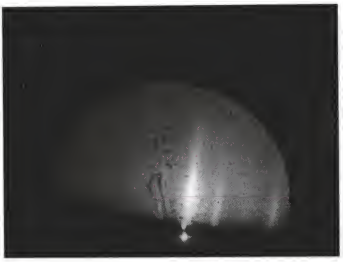


Figure A2.4 Illustration of the (1x3) (0001) surface of a hexagonal crystal. Arrows indicate the two crystal directions used to obtain the RHEED diffraction patterns. The "star" symbols are atoms on the surface and the "circle" symbols are atoms in the bulk.



(a)



(b)

Figure A2.5 RHEED images of (a) complete <11-20> direction and (b) incomplete <1-100> direction. Notice the extra lines in the <1-100> direction image from the missing rows of atoms.

APPENDIX 3
TEM SAMPLE PREPARATION

Sample preparation begins by cleaving thin strips of the material, about 1 cm long. These strips are glued together, using G-1 epoxy from Gatan, film side to film side. Other strips of sapphire are glued to add support, Figure A3.1. Tweezers are used to hold the strips together during the curing process to ensure thin glue lines. This stack of strips are polished using 320 grit SiC paper to create two parallel sides, perpendicular to the glue line. This is further polished using 600 grit SiC paper and a final polish with 3-5 micron diamond slurry on 800 grit SiC paper. The final thickness of the polished piece is 20 to 30 microns, Figure A3.2. This piece is glued to a nickel support grid, approximately 100mm thick, using the Gatan G-1 glue, Figure A3.3.

The sample is thinned further by using a Gatan Duo ion mill. The ion mill uses an argon ion beam accelerated toward the sample to remove material by collision. The settings of the ion mill are 5 kV and 0.7mA per beam. The milling angle is adjusted from a starting range of 18° to a final range of 13°. The ion mill uses two ion guns, 180° apart, for milling of both sides of the sample. The sample is also rotated to allow for a more uniform milling process. The final sample thickness is about 100nm.

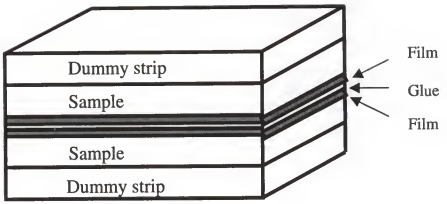


Figure A3.1 Strips of sample and support sapphire glued together into a sample stack.

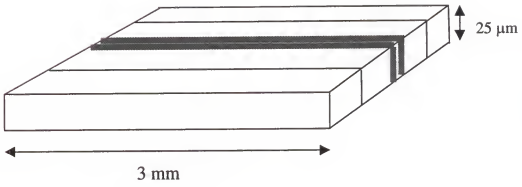


Figure A3.2 TEM sample polished to 25 μm thick.

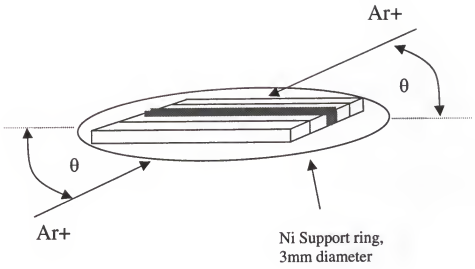


Figure A3.3 Illustrated is the sample glued to a 3mm Ni support ring and orientation of ion milling. Angle θ is the ion beam angle with respect to the plane of the sample.

REFERENCE LIST

1. M. Hong, M Passlack, J.P. Mannaerts, J. Kwo, S.N.G. Chu, N. Moriya, S.Y. Hou, V.J. Fratello, *Journal of Vacuum Science and Technology B*, **14(3)**, 2297 (1996)

2. F.Ren, M. Hong, W.S. Hobson, J.M. Kuo, J.R. Lothian, J.P. Mannaerts, J. Kwo, Y.K. Chen, A.Y. Cho, Tech. Dig. Int. Electron Devices Meeting, 943 (1996)

3. J. Kwo, D.W. Murphy, M. Hong, J.P. Mannaerts, R.L. Opila, R.L. Masaitis, A.M. Sergent, *Journal of Vacuum Science and Technology B*, **17(3)**, 1294 (1999)

4. J. Kwo, D.W. Murphy, M. Hong, R.L. Opila, J.P. Mannaerts, A.M. Sergent, R.L. Masaitis, *Applied Physics Letters*, **75(8)**, 1116 (1999)

5. L.W. Tu, Y.C. Lee, K.H. Lee, C.M. Lai, I. Lo, K.Y. Hsieh, M.Hong, *Applied Physics Letters*, **75(14)**, 2038 (1999)

6 A.R. Korton, M. Hong, J. Kwo, J.P. Mannaerts, N. Kopylov, *Physical Review B*, **60(15)**, 10913 (1999)

7. M. Hong, Z.H. Lu, J. Kwo, A.R. Korton, J.P. Mannaerts, J.J. Krajewski, K.C. Hsieh, L.J. Chou, K.Y. Cheng, *Applied Physics Letters*, **76(3)**, 312 (2000)

8. S. Nakamura, presented at 3rd International GaN Conference, Tokushima, Japan, October 1997

9. B.J. Baliga, *IEEE Electron Device Letters*, **10**, 455 (1989)

10. T.P. Chow, R. Tyagi, *IEEE Trans. Electron Devices*, **41**, 1481 (1994)

11. R.J. Trew, M.W. Shin, V. Gatto, *Solid-State Electron*, **41**, 1561 (1997)

12. M.N. Yoder, *IEEE Trans. Electron Devices*, **43**, 1633 (1996)

13. A.D. Bykhovski, B.I. Gelmont, M.S. Shur, *Journal of Applied Physics*, 81, 6332 (1997)

14. P.M. Asbeck, E.T. Yu, S.S. Lau, G.J. Sullivan, J. Van Hove, J. Redwing, *Electron. Letters*, **33**, 1230 (1997)

15. D.R. Askeland, *The Sciemce and Engineering of Materials*, 3rd ed., PWS, Boston MA, 1994

16. R. Wolfson and J.M. Pasachoff, *Physics*, Little, Brown and Company, Boston, 1987

17. W.M. Yim, E.J. Stofko, P.J. Zanzucchi, J.I. Pankove, M. Ettenburg, S.L. Gilbert, *Journal of Applied Physics*, **44**, 292 (1973)

18. V.W.L. Chin, T.L. Tansley, T. Osotchan, *Journal of Applied Physics*, **75**, 7365 (1994)

19. M.S. Shur, M.A. Khan, *Mat. Res. Bull.*, **22(2)**, 44 (1997)

20. A.I. Manakov, O.A. Esin, B.M. Lepinskikh, *Russian Journal of Physic and Chemistry*, **36**, 1481, (1965)

21. *Refractory Production, Handbook* [in Russian], Izd. Metallurgiya , 1965

22. G.W. Kaye, T.H. Laby, *Tables of Physical and Chemical Constants and some Mathematical Functions*, 11th ed, Longmans, New York, 1956

23. S.J. Pearton, *Int. J. Mod. Phys. B*, **7**, 4687 (1993)

24. M. Passlack, M. Hong, J.P. Mannaerts, *Applied Physics Letters*, **68**, 1099 (1996)

25. O. Kubaschewski and B. Hopkins, *Oxidation of Metals and Alloys* [Russian translated], Izd. Metallurgiya, 1965

26. S.S. Derbeneva, S.S. Batsano, *Dokl. Chem.*, **175**, 710 (1967)

27. S.S. Batsono, E.V. Dulepov, *Soviet Physics – Solid State*, **7(4)**, 995 (1965)

28. K.A. Gschneider, *Rare Earth Alloys* [Russian translation], Izd. Mir., 1965

29. Q. Xiao and J.J. Derby, *Journal of Crysal Growth*, **139,** 147 (1994)

30. C. T. Sah, *Fundamentals of Solid-State Electronics*, World Scientific, New Jersey, 1991

31. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition, Wiley, New York, 1981

32. D.R. Lide, *Handbook of Chemistry and Physics*, 71st edition, CRC Press, Boca Raton, 1990

33. R.L. Melik-Davtyan, N.F. Shvartsenau, A.I. Shelykh, *Inorganic Materials*, **2(1)**, 21 (1966)

34. J.L. Pentecost, *Ceramic Age*, **71**, 26 (1958)

35. A.A. Vorob'ev, *Physical properties of Crystalline Ionic Dielectrics* [in Russian], Izd. Tomsk. Univ. 1961

36. J. W. Mayer, S. S. Lau, *Electronic Materials Science,* Macmillan, New York, 1990

37. P. Neudeck, S. Kang, J. Petit, M. Tabib-Azar, *Journal of Applied Physics,* **75**, 12 (1994)

38. L.M. Terman, *Solid State Electronics,* **5**, 285 (1962)

39. J.N. Shenoy, G.L. Chindalore, M.R. Melloch, J.A. Cooper Jr., J.W. Palmour, K.G. Irvine, *Journal of Electronic Materials,* **24**, 303 (1995)

40. J. Shenoy, M.K. Das, J.A.Cooper Jr., M.R. Melloch, www.enc.purdue.edu/WBG/Basic_Measurments/MOS_Interface/Index.html (1998)

41. C-M Zetterling and M Ostling, Proceedings of ESSDERC'93, 497 (1993)

42. C-M Zetterling, PhD thesis for KTH, Royal Institute of Technology, Kista, Sweden (1997)

43. A. Golz, S. Gross, R. Janssen, E.G. Stein von Kamienski, H. Kurz, presented at ECSCRM'96 (1996)

44. X.W. Wang, T.P. Ma, G.J. Cui, T. Tamagawa, J.W. Golz, S. Karechi, B.H. Halpern, J.J. Schmitt, *Japanese Journal of Applied Physics,* **34**, 955 (1995)

45. S. Yoshida, S. Mizawa, Y. Fujii, S. Takada, H. Hayakawa, S.Gonda, A. Itoh, *Journal of Vacuum Science & Technology,* **16**, 990 (1979)

46. S. Stemmer, P. Pirouz, Y. Ikurhara, R.F. Davis, *Physical Review Letters,* **77**, 1797 (1996)

47. M.O. Aboelfotoh, R.S. Kern, S. Tanaka, R.F. Davis, C.I. Harris, *Applied Physics Letters*, **69**, 2873 (1996)

48. M. Stadele, J.A. Majewski, P. Vogl, *Physical Review B,* **56**, 6911 (1997)

49. V.M. Torres, M. Stevens, J.L. Edwards, D.J. Smith, R.B. Doak I.S.T. Tsong, *Applied Physics Letters,* **71**, 1365 (1997)

50. M. Lekova, G.W. Auner, F. Lin, R. Naik, V. Naik, *Materials Research Society Symposium Proceedings,* **449**, 245 (1997)

51. M.P. Thompson, A.R. Drews, C Huang, G.W. Auner, *MRS Internet Journal Nitride Semiconductor Research,* **4S1, G3.7** (1999)

52. K.A. Jones, P.B. Shah, K.W. Kirchner, R.T. Lareau, M.C. Wood, M.H. Ervin, R.D. Vispute, R.P. Sharma, T. Venkatesan, O.W. Holland, *Materials Science & Engineering,* **B61-62**, 281 (1999)

53. H.C. Casey Jr, G.G. Fountain, R.G. Alley, B.P. Keller, S.P. Denbaars, *Applied Physics Letters,* **68**, 1850 (1996)

54. M. Sawada, T. Sawada, Y. Yamagata, K. Imai, H. Kumura, M. Yoshino, K. Iizuka, H. Tomozawa, *Proceedings of the Second international conference on Nitride Semiconductors*, Tokushima, 482 (1997)

55. S. Aurlkumaran, T. Egawa, H. Ishikawa, T. Jimbo, M. Umeno, http://ojps.api.org/journals/doc/APPLAB-ft/vol_73/iss_6/809_1.html (1998)

56. S.C. Binari, K. Doverspike, G. Kelner, H.B. Dietrich, A.E. Wickenden, *Solid State Electronics,* **41**, 177 (1997)

57. B. Gaffey, G. Chong, L. Guido, X.W. Wang, T.P. Ma, *to be published*

58. F. Ren, C.R. Abernathy, J.D. MacKenzie, B.P. Gila, S.J. Pearton, M. Hong, M.A. Marcus, M.J. Schurman, A.G. Baca, R.J. Shul, *Solid State Electronics,* **42**, 2177 (1998)

59. H. Kawai, M. Hara, F. Nakamura, T. Asatsuma, T. Kobayashi, S. Imanaga, *Journal of Crystal Growth,* **189/190**, 738 (1998)

60. S.D. Wolter, B.P. Luther, D.L. Waltemyer, C. Onneby, S.E. Mohney, R.J. Molnar, *Applied Physics Letters,* **70**, 2156 (1997)

61. S.D. Wolter, S.E. Mohney, H. Venugopalan, A.E. Wickenden, D.D. Koleske, *Journal of the Electrochemical Society,* **145**, 629 (1998)

62. E.D. Readinger, S.D. Wolter D.L. Waltemyer, J.M. Delucca, S.E. Mohney, B.I. Prenitzer, L.A. Gainnuzzi, R.J. Molnar, *Journal of Electronic Materials,* **28**, 257 (1999)

63. M. Hong, J.P. Mannaerts, J.E. Bower, J. Kwo, M. Passlack, W-Y. Hwang, L.W. Tu, *Journal of Crystal Growth,* **175/176**, 422 (1997)

64. F. Ren, M. Hong, W.S. Hobson, J.M. Kuo, J.R. Lothian, J.P. Mannaerts, J. Kwo, S.N.G. Chu, Y.K. Chen, A.Y. Cho, *Solid State Electronics,* **41**, 1751 (1997)

65. Y.C. Wang, M. Hong, J.M. Kuo, J.P. Mannaerts, J. Kwo, H.S. Tsai, J.J. Krajewski, J.S. Weiner, Y.K. Chen, A.Y. Cho, *Materials Research Society Symposium Proceedings,* **573**, 219 (1999)

66. J. Kwo, M. Hong, A.R. Kortan, D.W. Murphy, J.P. Mannaerts, A.M. Sergent, Y.C. Wang, K.C. Hsieh, *Materials Research Society Symposium Proceedings,* **573**, 57 (1999)

67. T.S. Lay, M. Hong, J. Kwo, J.P. Mannaerts, W.H. Hung, D.J. Huang, *Materials Research Society Symposium Proceedings,* **573**, 131 (1999)

68. A.R. Mortan, M. Hong, J. Kwo, J.P. Mannaerts, N. Kopylov, *Materials Research Society Symposium Proceedings,* **573**, 21 (1999)

69. M. Hong, K.A. Anselm, J. Kwo, H.M. Ng, J.N. Baillargeon, A.R. Koetan, J.P. Mannaerts, A.Y. Cho, C.M. Lee, J.I. Chyi, T.S. Lay, *to be published* (1999)

70. F. Ren, M. Hong, S>N>G> Chu, M.A. Marcus, M.J. Schurman, A. Baca, S.J. Pearton, C.R. Abernathy, *Applied Physics Letters,* **73**, 3893 (1998)

71. F. Ren, M. Hong, J.P. Mannaerts, J.R. Lothian, A.Y. Cho, *Journal of Electrochemical Society,* **144**, L239 (1997)

72. *JEOL NEWS*, JEOL News Editorial Board, JEOL LTD, Akishima, Tokyo, Japan

73. B.D. Cullity, *Elements of X-ray Diffraction*, 2nd ed, Addison-Wesley, London, 1978

BIOGRAPHICAL SKETCH

Brent Paul Gila was born in the small town of Vero Beach on the Atlantic coast of Florida. After graduating from Vero Beach High School in June 1988, he began attending college at the illustrious University of Florida in the fall of 1988. It was here that his love for college football began. Brent entered the materials science department in summer of 1990. During his undergraduate studies, he began working under the supervision of Dr. Augusto Morrone in the field of transmission electron microscopy and Dr. Anthony Brennan in the field of light cured resins for dental applications. He received his bachelor's degree in the spring of 1994 with specialties in polymer and electronic materials and also received a minor in statistics. Brent immediately began graduate school at the University of Florida under the supervision of Dr. Robert M. Park studying molecular beam epitaxy crystal growth of II-VI materials and light emitting diode structures. This continued until his interest in this field was depleted, along with his funding, in the summer of 1997. He was plucked form the depths of unemployment by Dr. Cammy Abernathy and began research on dielectric materials. Under Dr. Abernathy's supervision, Brent assembled a molecular beam epitaxy system for oxide growth and completed the research found in this dissertation. Post graduation plans are to continue research on these dielectric materials as a post-doc under Dr. Abernathy and apply to the National Aeronautics and Space Administration for the position of astronaut.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Cammy R. Abernathy, Chairperson
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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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